

CROC_Final

Supply voltage :

VDD (Core) = 2V5

VDDP (I/O Ring) = 3V3

I/O used : 334/344

Header_Detection_FEB

(1b for each FEB) (From FEPGA)

(Voltage I/O : 3V3)

From TTCrq Mezzanine

(Channel B, Brcst_Strobe1, L0, Clk)

(Voltage I/O : ???)

N_Read_From_SPY

(To All FEPGA)

(Voltage I/O : 3V3)

End_Of_Transfert FEB to FEPGA

(1b for each FEPGA)

(Voltage I/O : 3V3)

Data_Spyed

(data 21b, Ctrl word 2b)

(Voltage I/O : 3V3)

IN_Lemo_Spare

Ext_Clk

Ext_Trig (ChanB, L0)

(Voltage I/O : 3V3)

SPECS

(Data 16b, Add 8b, Rd, Wr, Irq)

(Voltage I/O : 3V3)

Spy_Data_Add

(9 bit Add, 2 Sel PGA, 2 SEL Feb)

(Voltage I/O : 3V3)

Ext_Event_Counter

(Nicomatic : 4 In, 4 Out)

(Voltage I/O : 3V3)

Extra_information

From_BckPlan6U

Crate_Id_From_Bckplane

(Voltage I/O : 3V3)

Board_Id_From_Bckplane

(Voltage I/O : 3V3)

Spy_PGA_Identify

SPY_PGA
APA450 PBGA456

344 User I/Os

48 Embedded RAM Blocks (256x9)

Ctrl_To_Optical_Transmitter

(Voltage I/O : 3V3)

(Reset_Laser1, Fault1, TxEnLaser1, TxDisLaser1, Reset_Laser2, Fault2, TxEnLaser2, TxDisLaser2, CAV/Tx_er[0 to 7], Reset_ChipGOL_board1, DAV/Tx_en[0 to 7], Ready_ChipGOL[0 to 7], CAV/Tx_er[8 to 15], Reset_ChipGOL_board2, DAV/Tx_en[8 to 15], Ready_ChipGOL[8 to 15], ON/OFF_Clk_Bd1, ON/OFF_Clk_Bd2, Bd1_Select_DiffA, Bd1_Select_DiffB, Bd2_Select_DiffA, Bd2_Select_DiffB)

OUT_To_Led

Header, EndTransf_FEBtoFEPGA, Transf_FEBtoSPY, New_Seq_DumpSpy.L0_Trigger, Reset_All

(Voltage I/O : 3V3)

OUT_New_Seq_Dump_Spy

(Voltage I/O : 3V3)

OUT_Lemo_Spare

(Voltage I/O : 3V3)

OUT_Trig_Seq_L0

(Voltage I/O : 3V3)

N_Reset_All

(Voltage I/O : 3V3)

Spare_From_SPY_PGA

(Voltage I/O : 3V3)

Spare_To_Pastille and ConScop

(Voltage I/O : 3V3)

N_Reset

(DelayChip, TTCrq, All_FEPGA)

(Voltage I/O : 3V3)

Clk_Div

(Voltage I/O : 3V3)

Clk

(Clk_Board_To_FEPGA, Clk_Board_To_Delay_Chip, Clk_Board_To_Lemo, Clk_Board_To_SPECS)

(Voltage I/O : 3V3)

Clk_Board

(Voltage I/O : 3V3)

Channel_B_To_backplane

(Voltage I/O : 3V3)

L0_To_backplane

(Voltage I/O : 3V3)

(1 for Lemo and another for backplane)

Crate_Identifier

(Voltage I/O : 3V3)

Board_Identifier

(Voltage I/O : 3V3)

(Sortance

CrateID ???)

Extra_information

To_Optical_Transmitter

N_Delatch_from_backplane

(Voltage I/O : 3V3)

N_Delatch_from_CROC

CROC_Prototype_v3

I/O SPYPGA