Un réseau Ethernet de mille et un capteurs intelligents pour l'expérience OPERA

***IPNL** Institut de **P**hysique Nucléaire de **L**yon*

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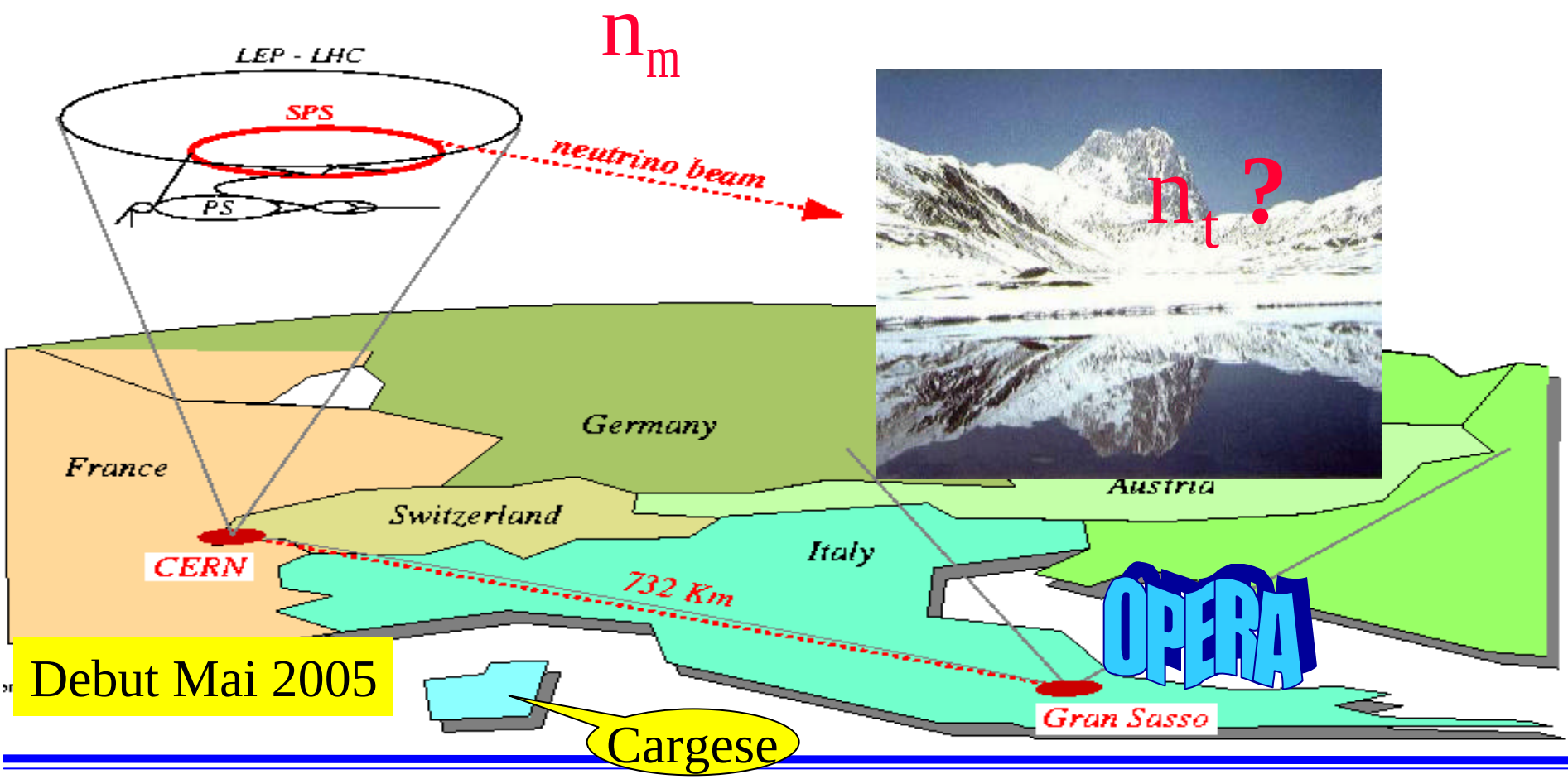
+ K.Korcyl, P.Golonka, Cracow, ATLAS HLT modeling

Programme

- OPERA
- Description du nœud de base:
  - Ethernet capable front-end
- Premiers travaux sur le réseau

CERN to Gran Sasso Neutrino Beam



COLLABORATION

29 groupes
~ 130 physiciens

Belgium

China

CERN

Croatia

France

Annecy, Lyon, Orsay, Strasbourg

Germany

Israel

Italy

Bari, Bologna, Frascati, Naples, Padova, Rome, Salerno

Japan

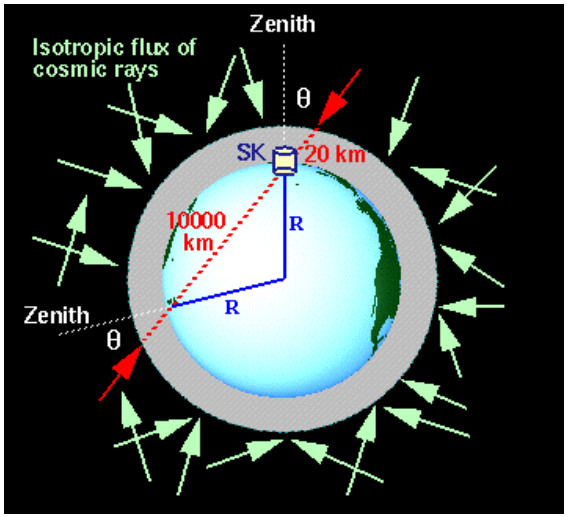
Aichi, Toho, Kobe, Nagoya, Utsunomiya

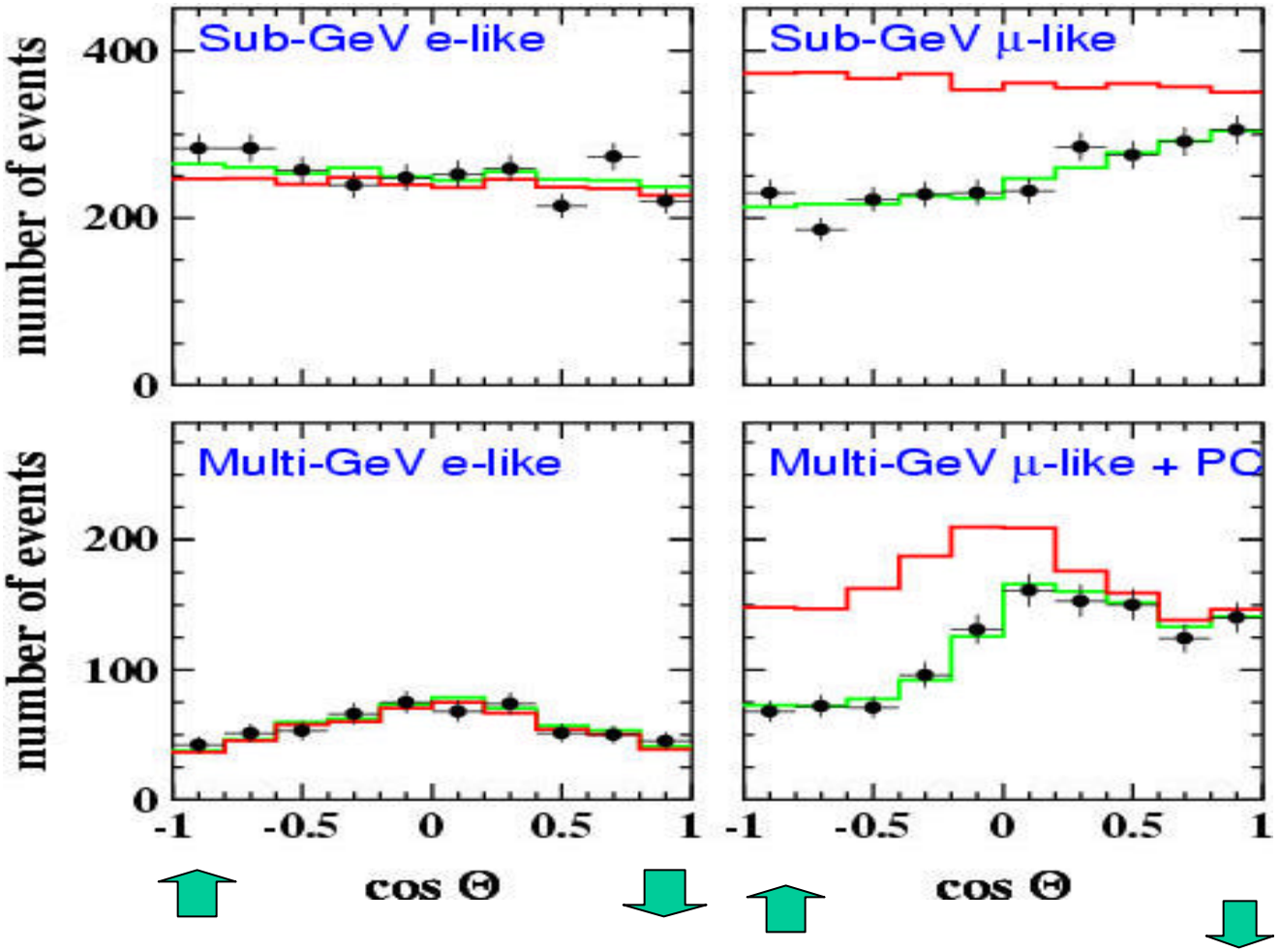
Switzerland

Turkey

Russia

Le signal de SuperK
Les ν_μ devaient être symétriques haut-bas. Ils ne le sont pas

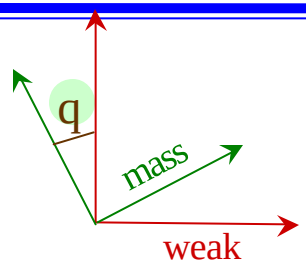




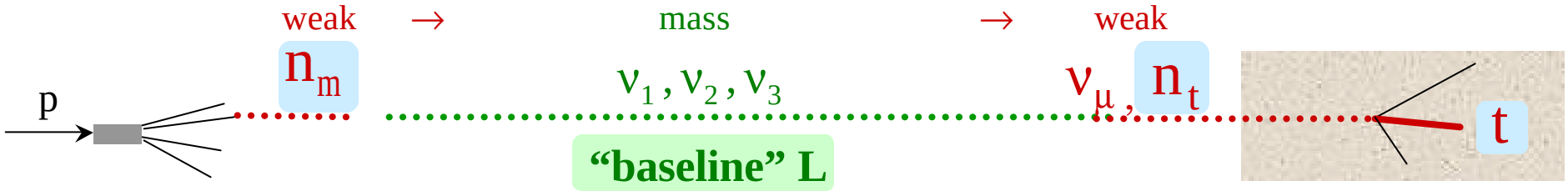
La solution du puzzle: oscillation neutrino

✸ **"Mixed" eigen-states** { interactions: **"weak" e.s.** (n_e, n_m, n_t)
propagation : **"mass" e.s.** (n_1, n_2, n_3)

"invisible"



✸ **Quantum Mechanics**

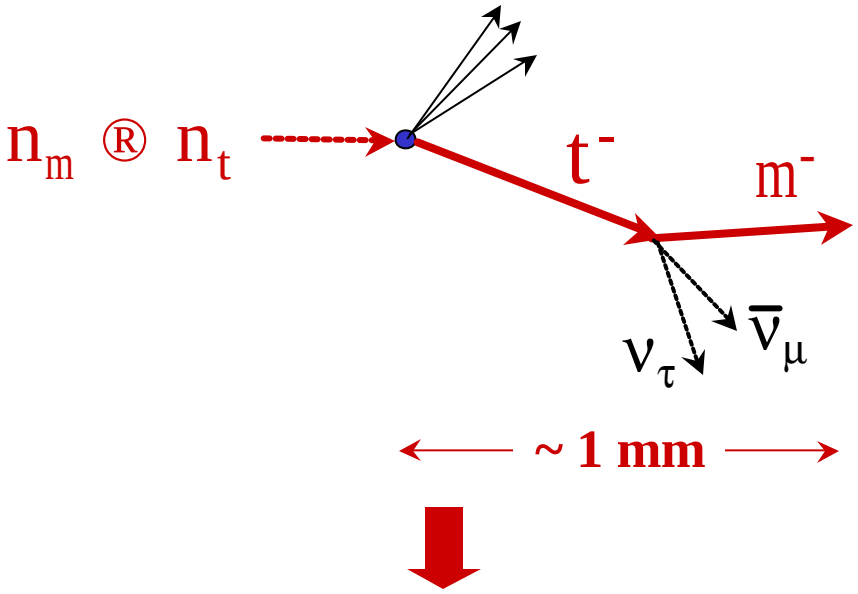


n_m **production**

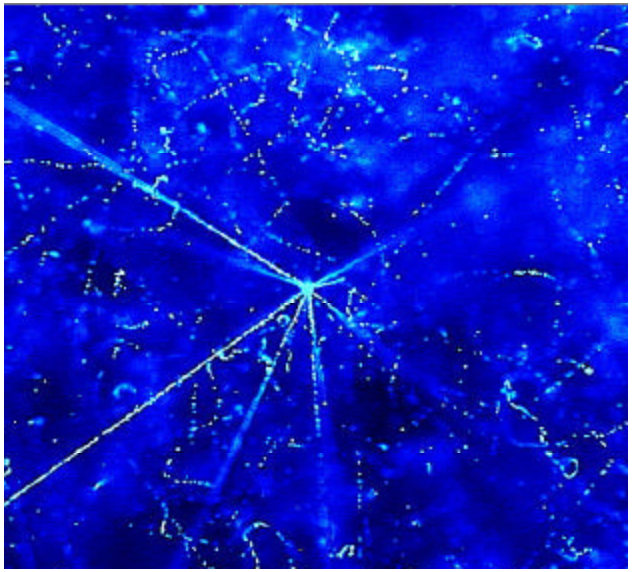
Dm^2_{ij} ® **different** propagation of ν_i waves
® **different** ν_i mixture at detector
® **not only** ν_μ at detector !

n_t **detected**, although ν_μ was produced !

But d ’OPERA

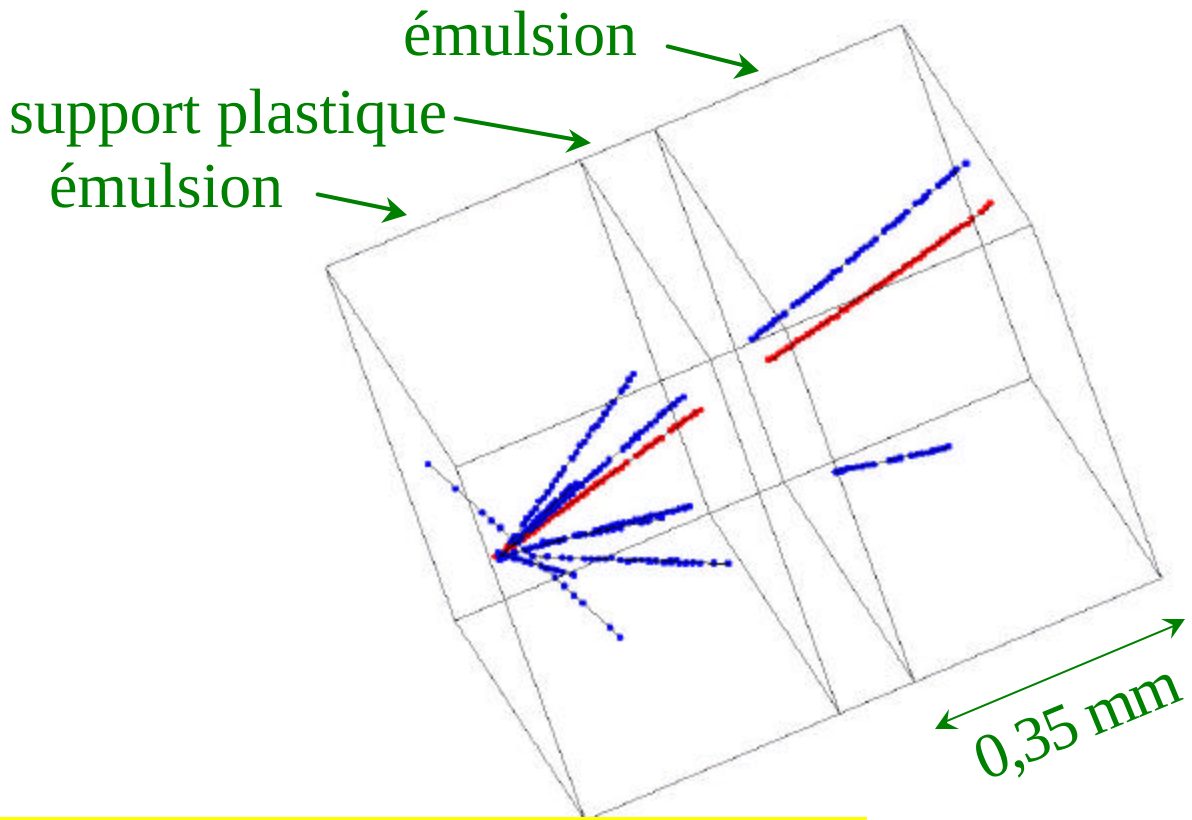


Trouver la trace “cassée”, résultant de la désintégration du τ



Interaction des ν_μ dans les émulsions photographiques
(une “tranche tomographique”)

Evénement, dans l'émulsion, puis reconstruit en trois dimensions par ordinateur



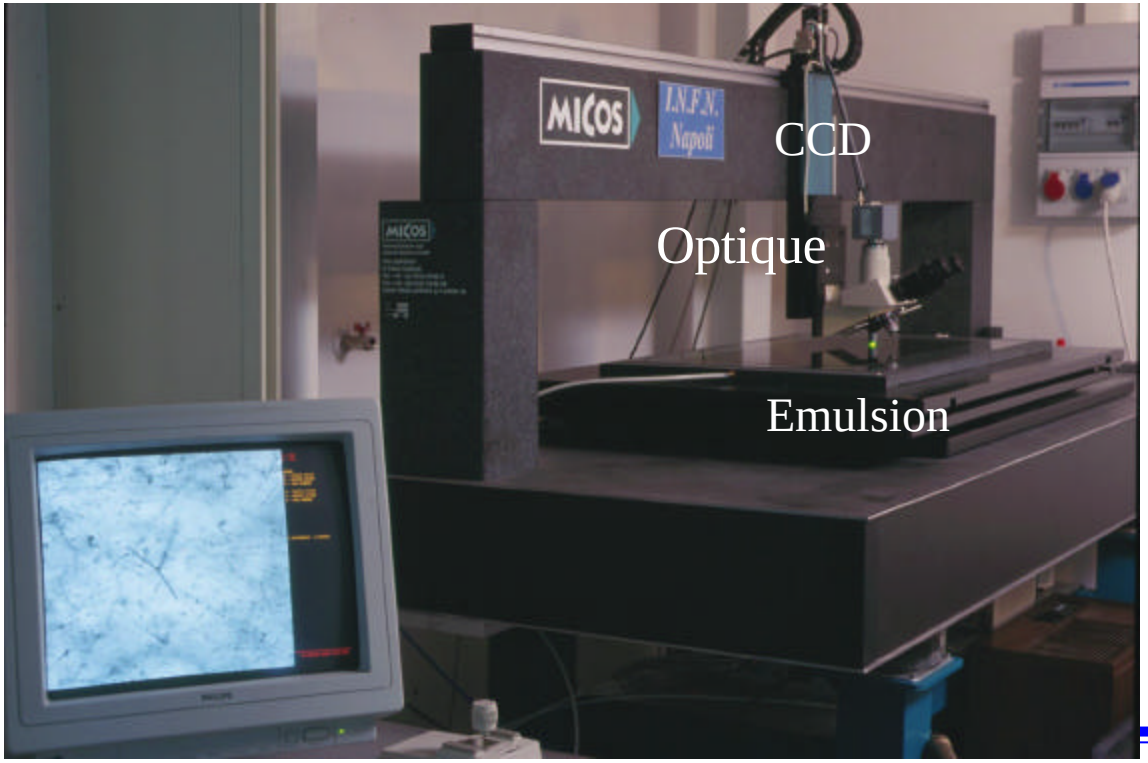
200000 m2 d émulsion ~ 0.5 Giga clichés de photo

Visualisation par ordinateur des trajectoires de particules dans deux couches d'émulsions disposées de part et d'autre d'un support plastique

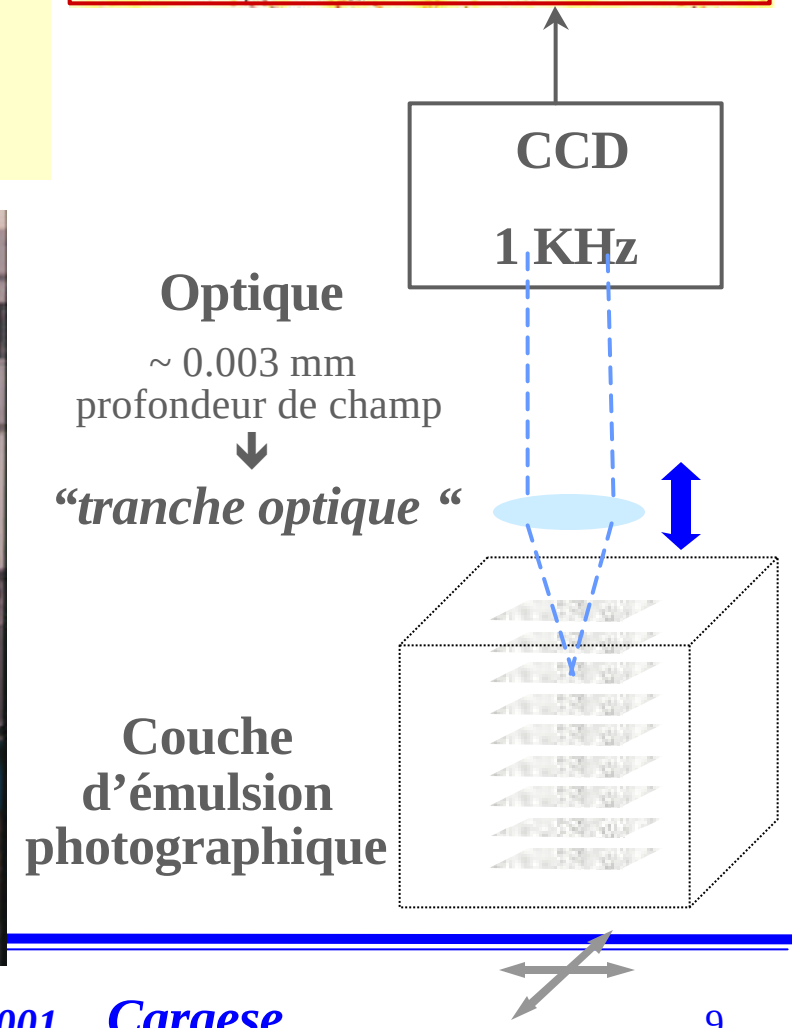
Microscope pour analyser automatiquement les images en trois dimensions

Entièrement controlé par ordinateur

UTS (1cm*2*/h) ==> SUTS (20 cm*2*/h), x 20stations



Interaction des n_t visualisée en 3 dimensions, en faisant des séries d'images "en tranches "



	Track density In emulsion	Scan area
CHORUS	**10k /cm^2**	**60 k cm^2**
DONUT	**100k /cm^2**	**20 k cm^2**
OPERA	**100 /cm^2**	**5 M cm^2**

DONUT ECC:
5 x 5 mm^2 times 8 cells:

100000 track segments;

⇩

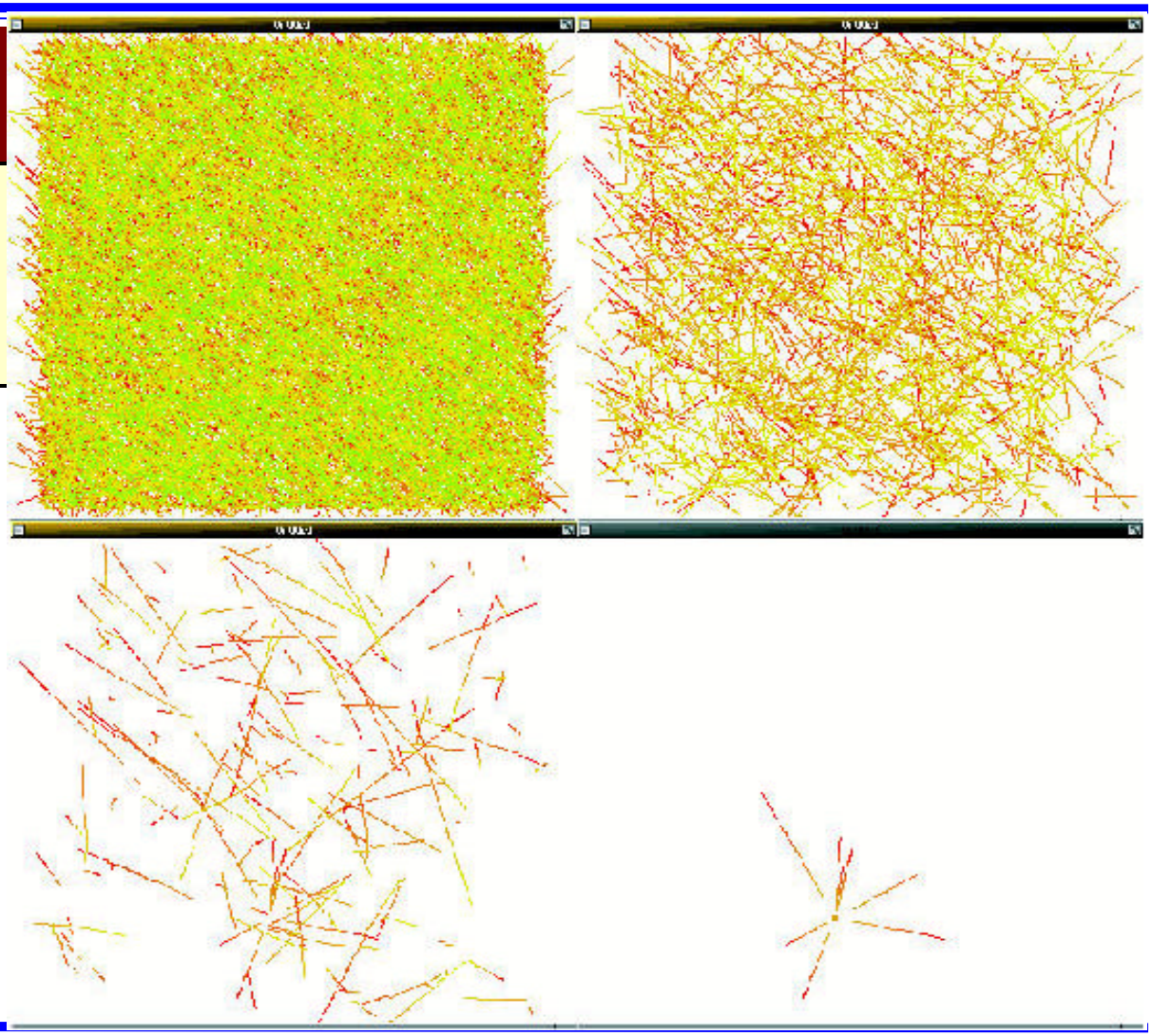
900 stopping tracks;

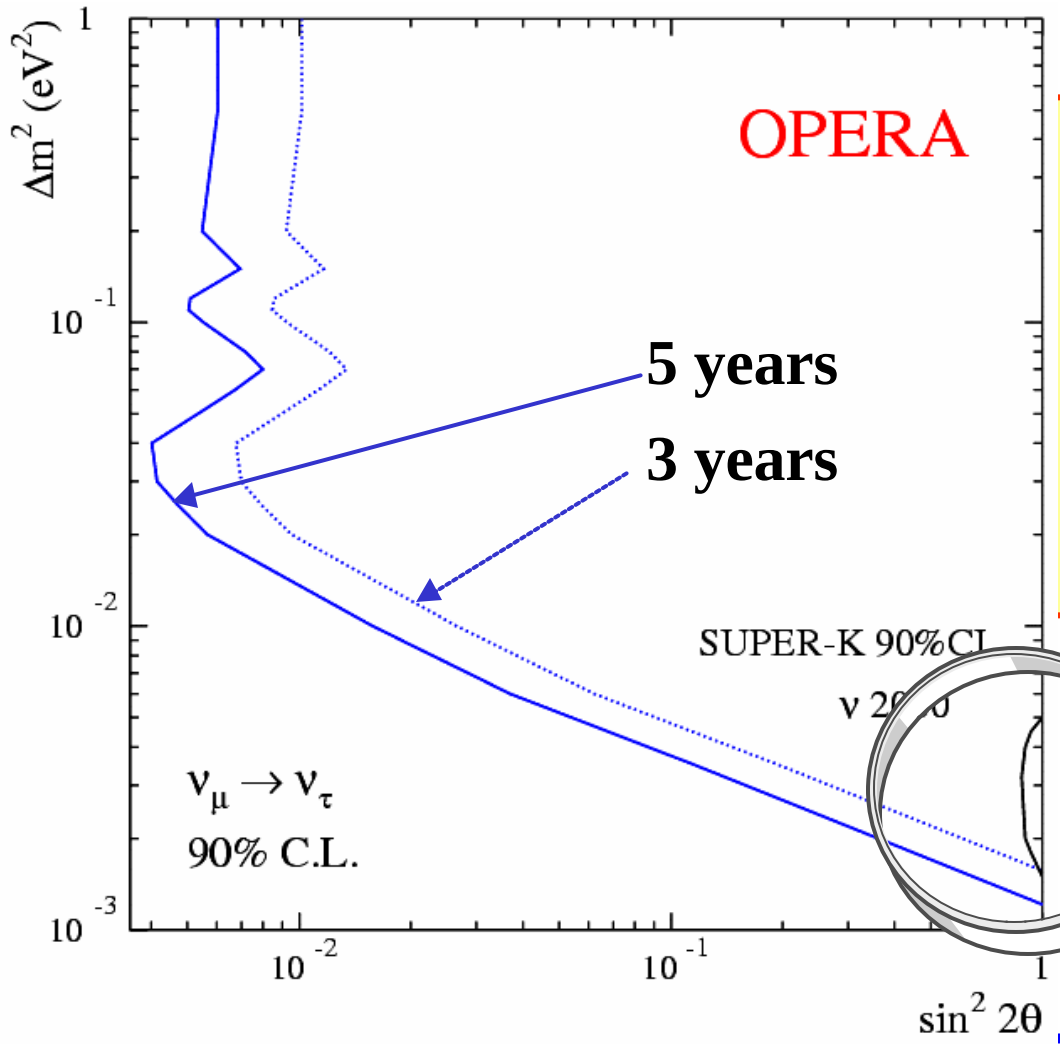
⇩

180 small angle, high energy;

⇩

1 neutrino interaction
(require low IP tracks)



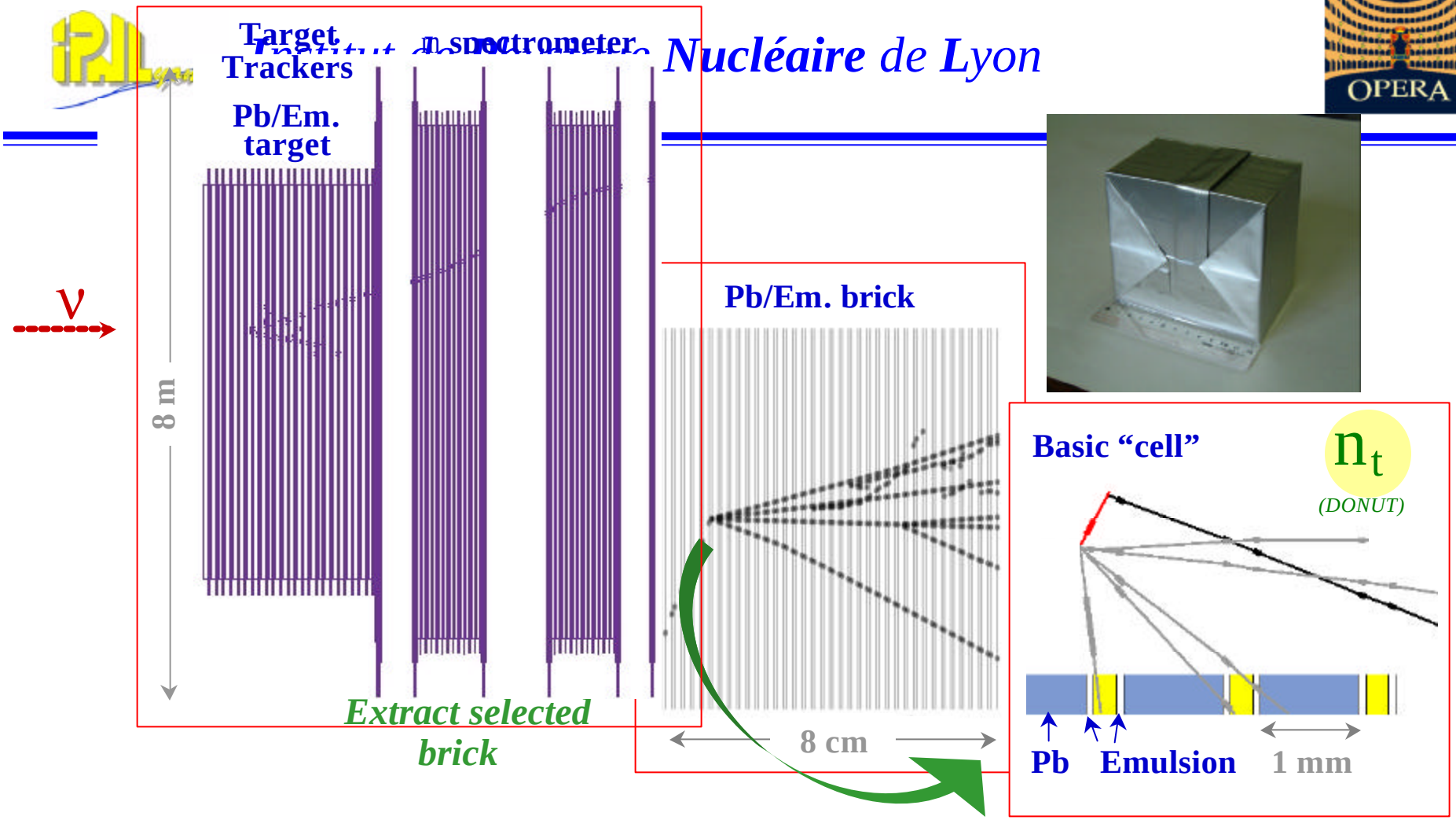


t **decay**	Δm^2 (10^{-3} eV^2)			**b.g.**
	1.5	3.2	5.0	
e	1.7	7.7	18.5	0.19
m	1.3	5.7	13.8	0.13
h	1.1	4.9	11.8	0.25
Total	**4.1**	**18.3**	**44.1**	**0.57**

n_t **events**

Dm^2 = 1.2×10^{-3} eV^2
at full mixing

$\sin^2(2q)$ = 6.0×10^{-3}
at large Dm^2



Electronic detectors

→ select n interaction brick

→ m ID, charge and p

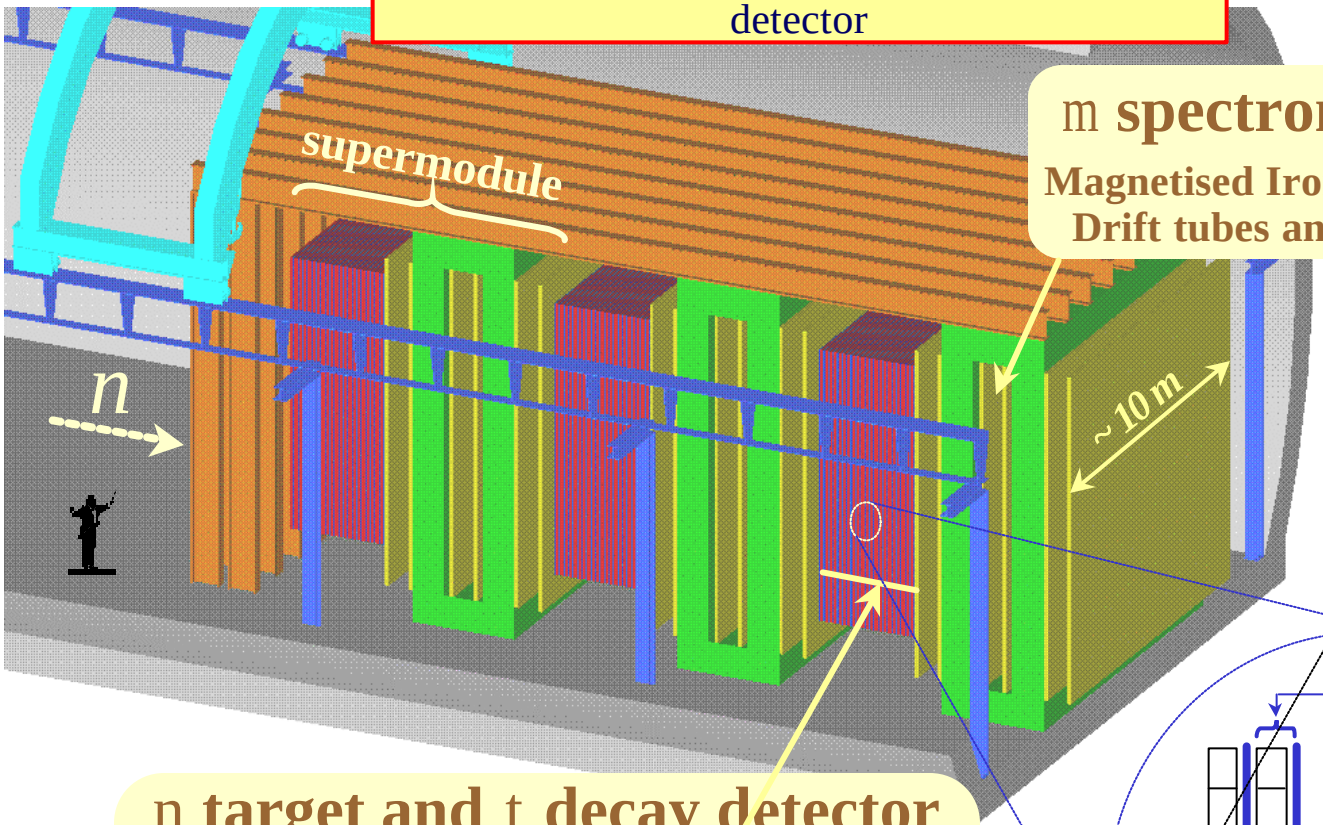
Emulsion scanning

® vertex search

→ decay search

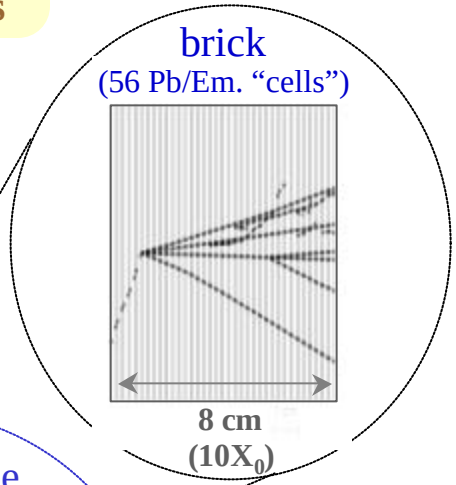
→ e/g ID, kinematics

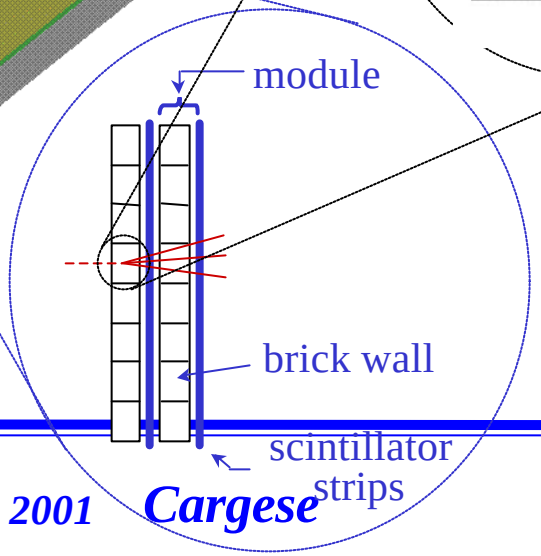
The OPERA detector at Gran Sasso a hybrid detector



m spectrometer

Magnetised Iron Dipoles
Drift tubes and RPCs





n target and t decay detector

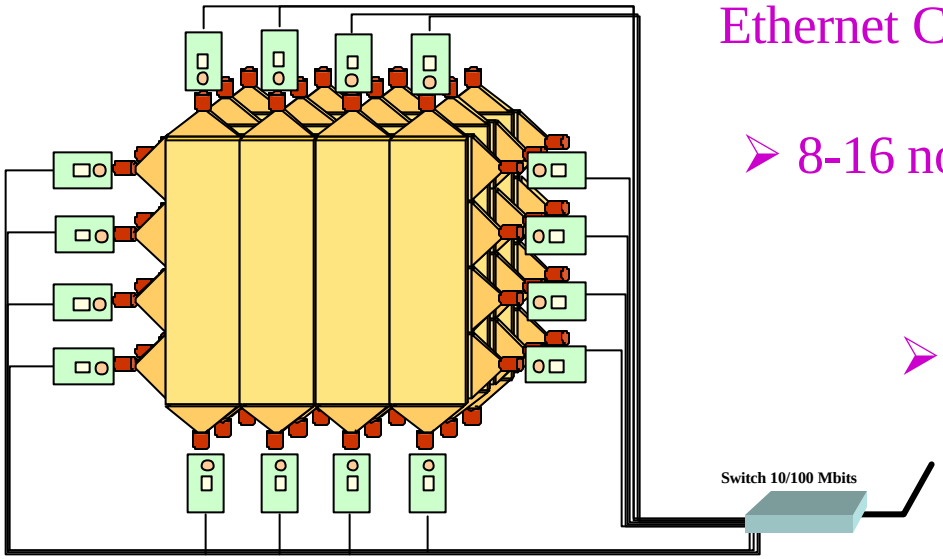
3 "supermodules" each one is a sequence of 24 "modules" consisting of

- a "wall" of Pb/emulsion "bricks"
- 2 planes of orthogonal scintillator strips

IPNL proposal for the OPERA DAQ

- Distributed acquisition system on Ethernet

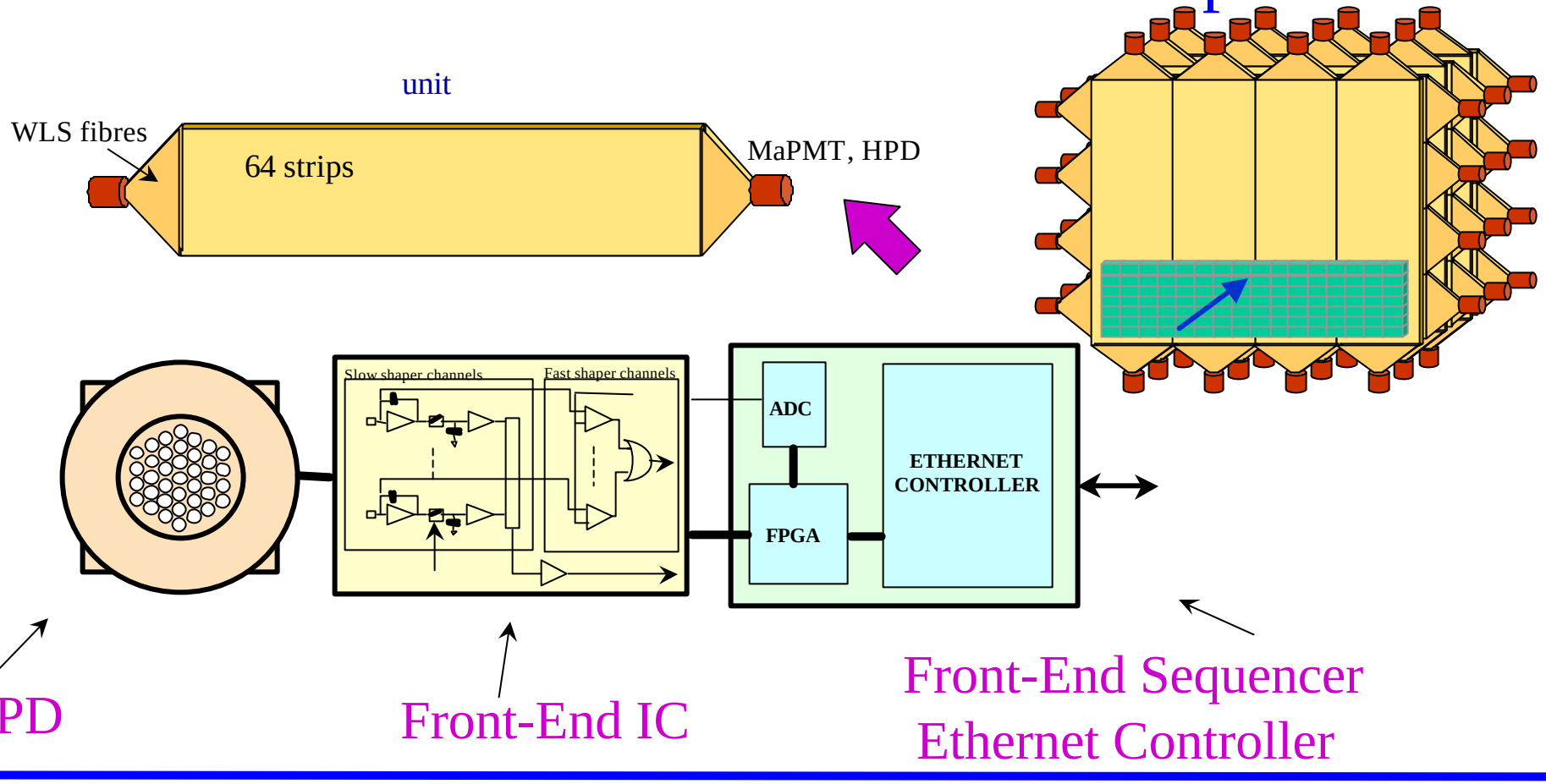
- Smart sensors also called
  Ethernet Capable Front-end Module

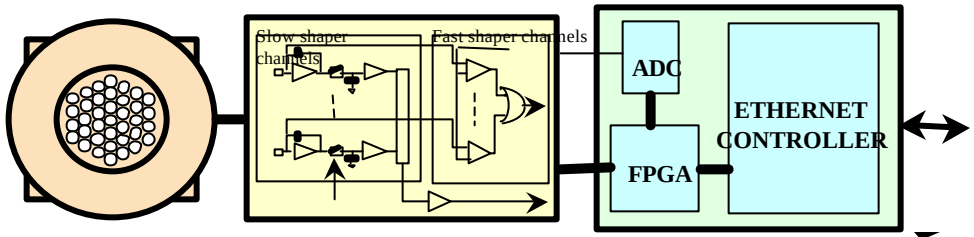


- 8-16 nodes per plane data rate of 8 Mbits/plane

- A network tree architecture with a two levels of switches up to the event building work station

Ethernet Front-End Module concept





HPD

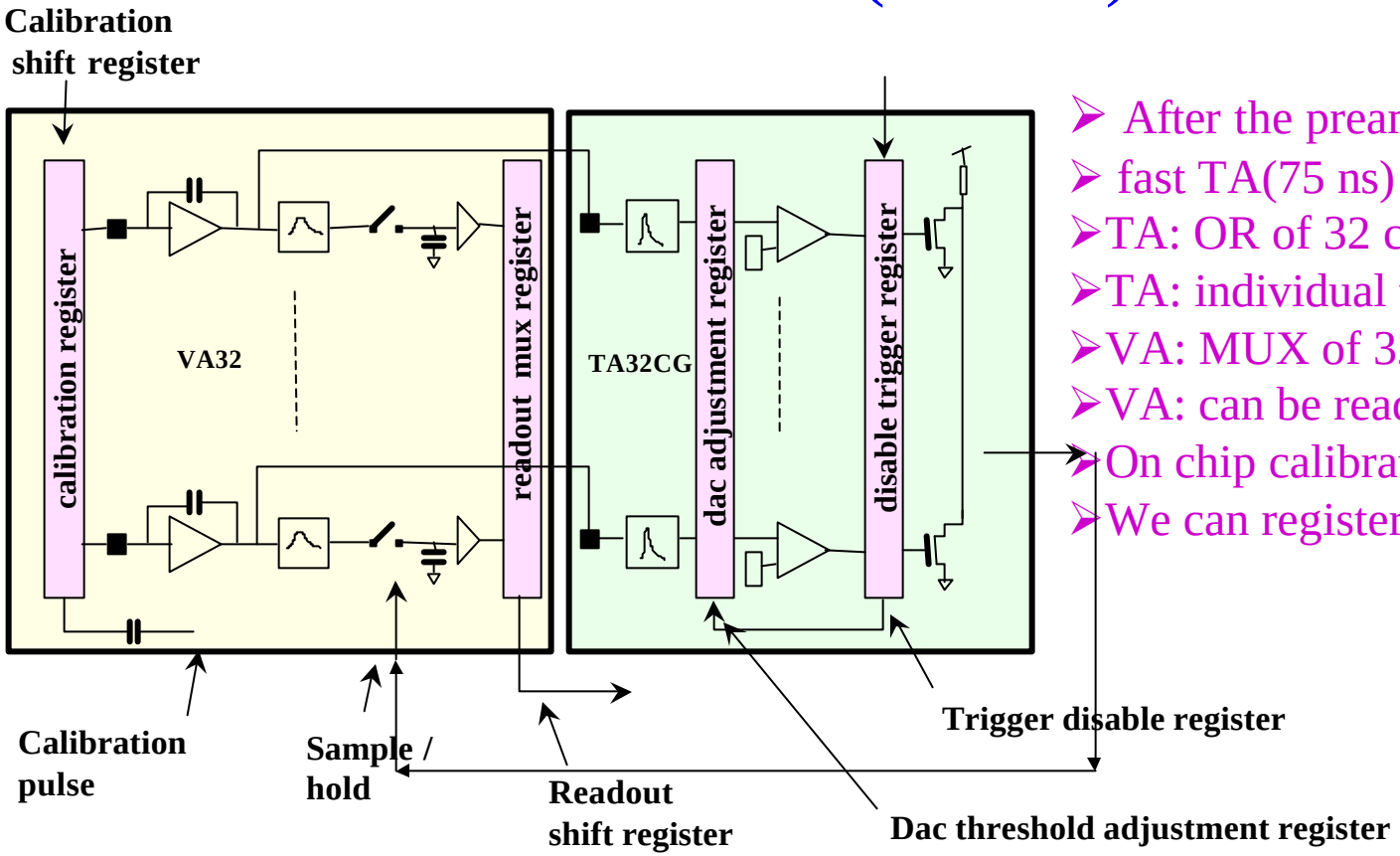
Front-End IC

Front-End Sequencer
Ethernet Controller

- **Concept of Ethernet smart sensor** :
  - Control of the multi-channel Front-End chip
  - Sequence the readout ***(FPGA)***
  - Send the data through Ethernet network ***(Ethernet controller)***

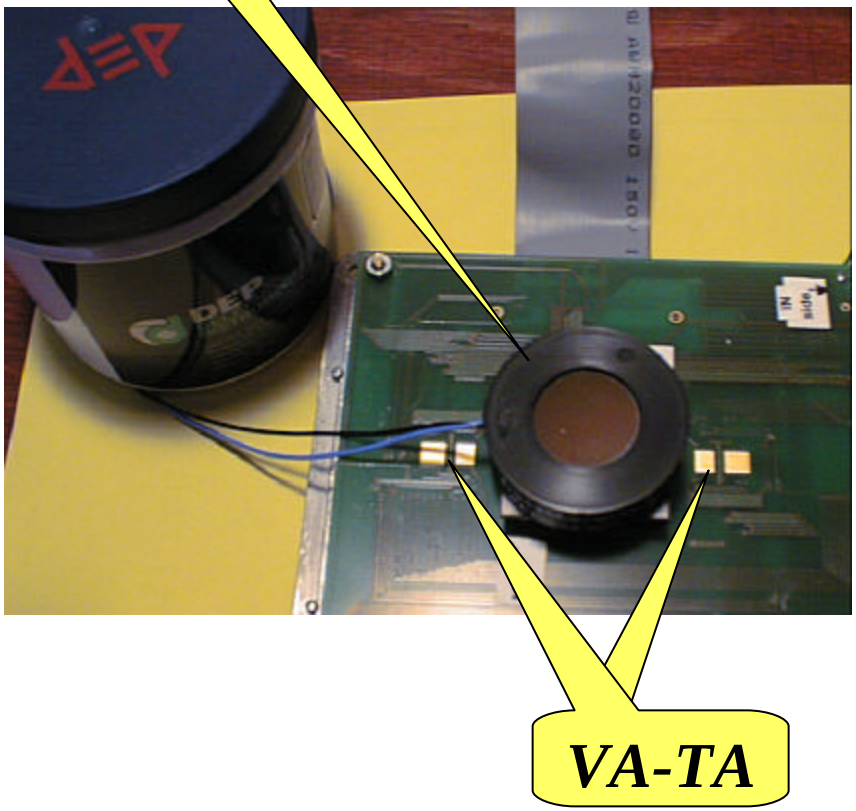
- **Access *(any application able to open a socket on the network)*** :
  - Any WEB browser
  - LabVIEW interface through Ethernet
  - C program interface
- **Each F.E. element (ex. 1 HPD) is a *node* on the network *(no BUS)***

Electronics: the Front-end chip VA-TA32CG (IDEAS)

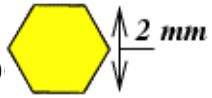


- After the preamp -->2 paths
- fast TA(75 ns) / slow VA (1-3 µs)
- TA: OR of 32 channels --> S/H
- TA: individual thresholds
- VA: MUX of 32
- VA: can be read at 100 ns/channel
- On chip calibration i
- We can register extra triggers

HPD-VATA system



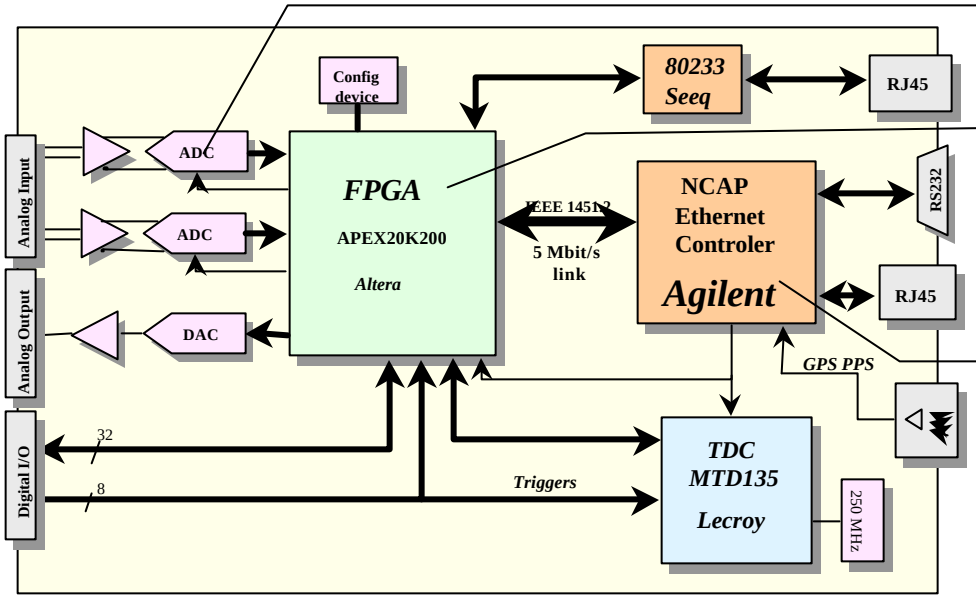
➢ **HPD general characteristics :**

- ❑ 61 pixels
- ❑ S20 photo  3 mm ∅
- ❑ QE : 15 % (520 nm)
- ❑ gain (10 kV) : 3000 e^- (0.5 fC/p.e.)

➢ **HPD-VATA performance :**

- ❑ auto-triggerability at single p.e.
- ❑ p.e. resolution (> 7 peaks)
- ❑ gain uniformity ~ 5 %
- ❑ cross-talk ~ 2 %
- ❑ p.e. resolution HV_{min} = 5 kV
- ❑ gain linearity with HV
- ❑ Dark Current ~1 kHz / pixel
- ❑ dynamic range ~ 200 p.e.

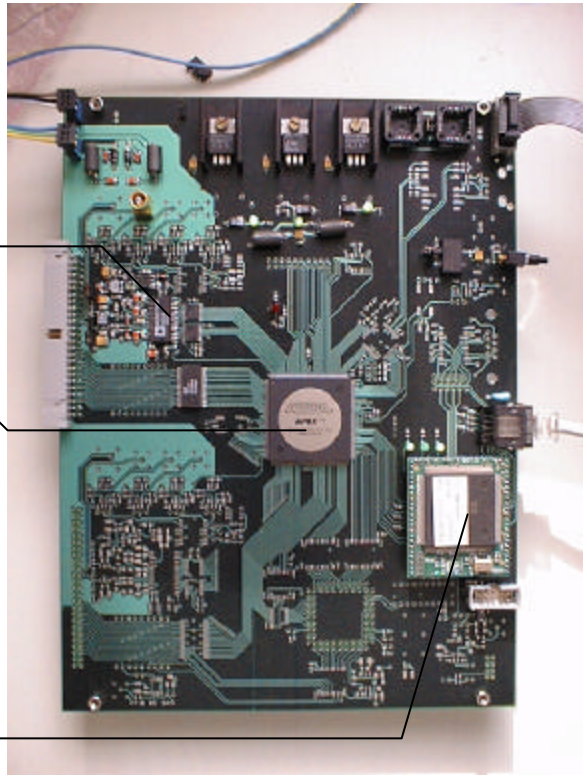
First prototype using an Ethernet Controller from Agilent (BFOOT 11501)



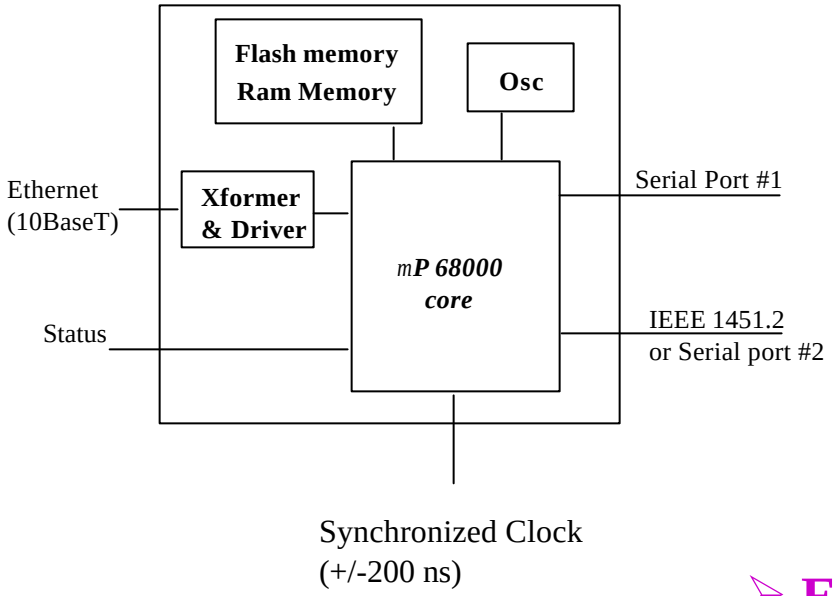
ADC

FPGA

Ethernet Controller



BFOOT 11501 features

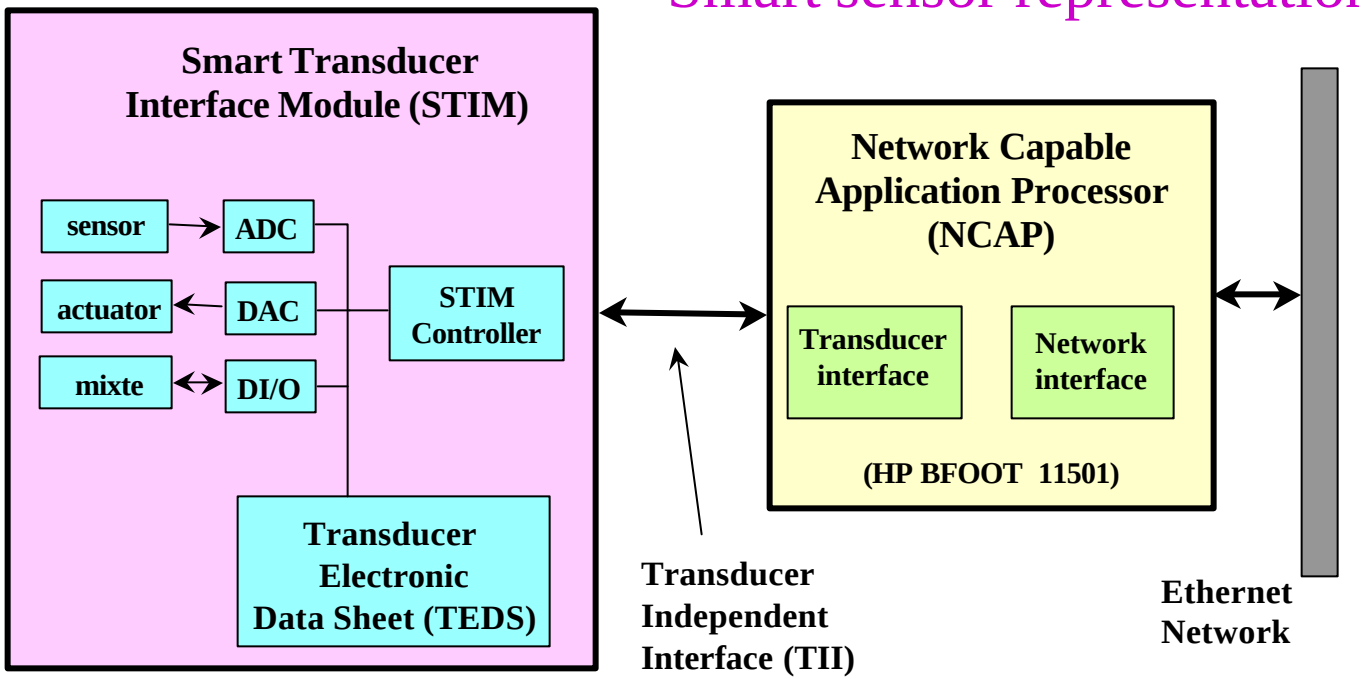


- Custom ASIC with a processor core.
- Embedded Ethernet controller.
- Time stamping function with a Synchronization capibility of +/- 200 ns accuracy.

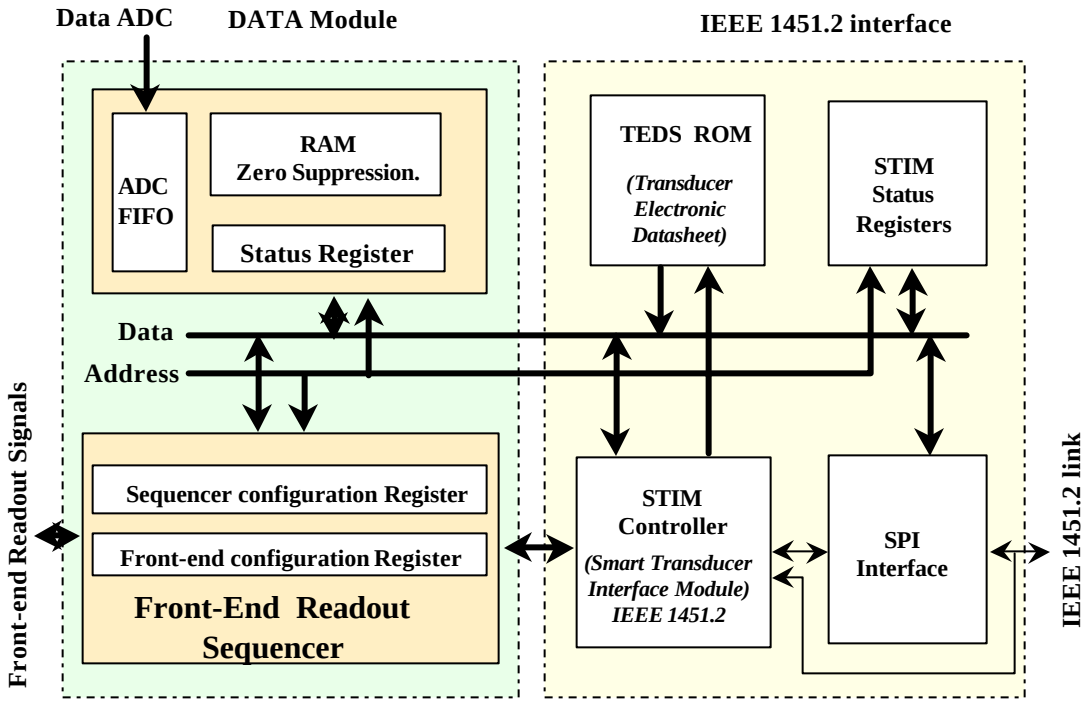
- **Embedded web server, HTML et Java.**
- **IEEE 1451.2 standard.**

IEEE 1451.2 concept

Smart sensor representation

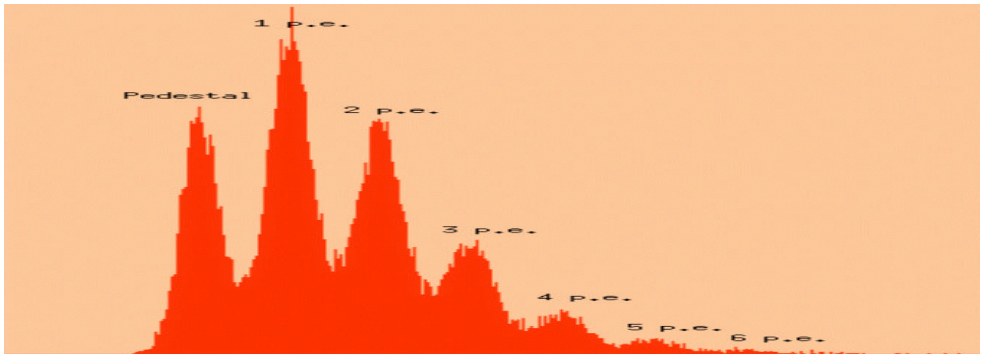


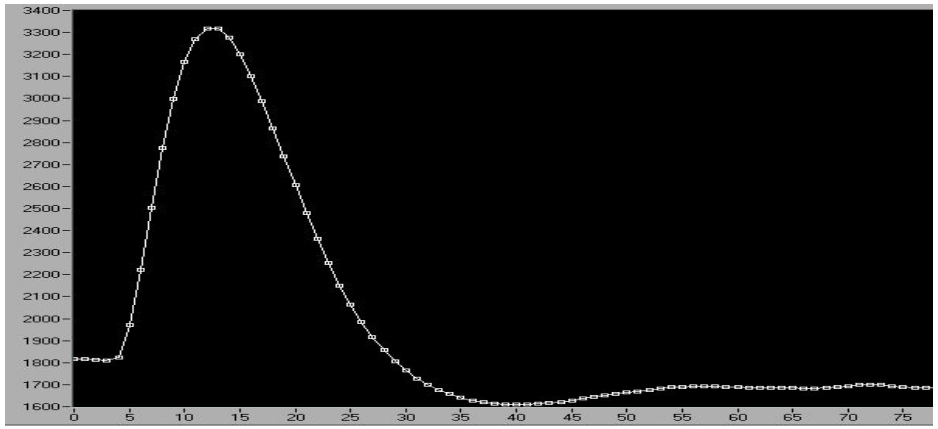
FPGA implementation of a STIM in VHDL langage



- IEEE 1451.2 interface
- The event channel is implemented in a FIFO
- A zero suppression is possible
- Front-end readout sequencer and controller.

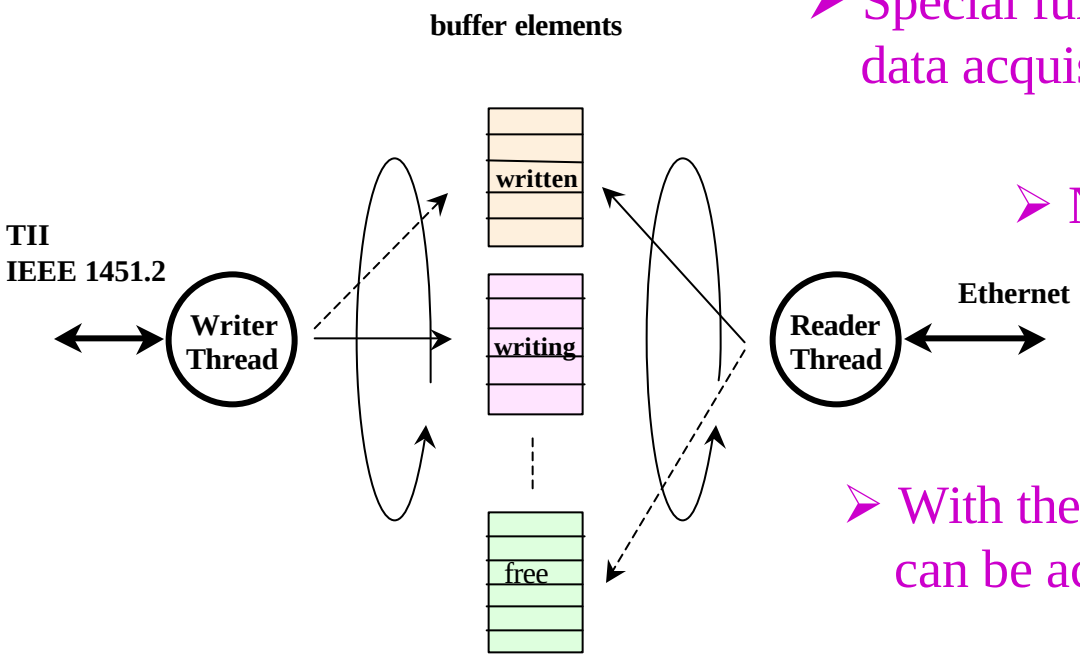
Read access mode through a JAVA applet





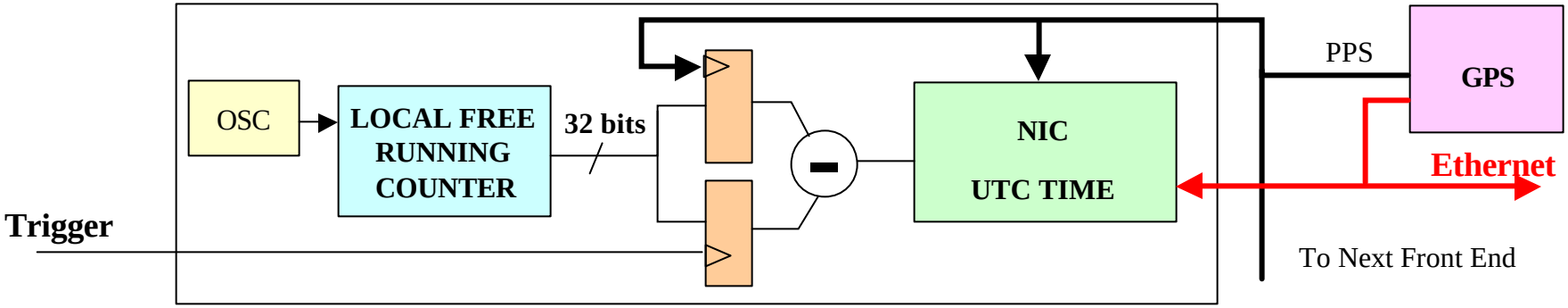
- The ADC data are continuously readout through Ethernet.
- WEB Oscilloscope !!!!
- Usefull for monitoring and slow control through simple commands: e.h http://lyotmp9/...

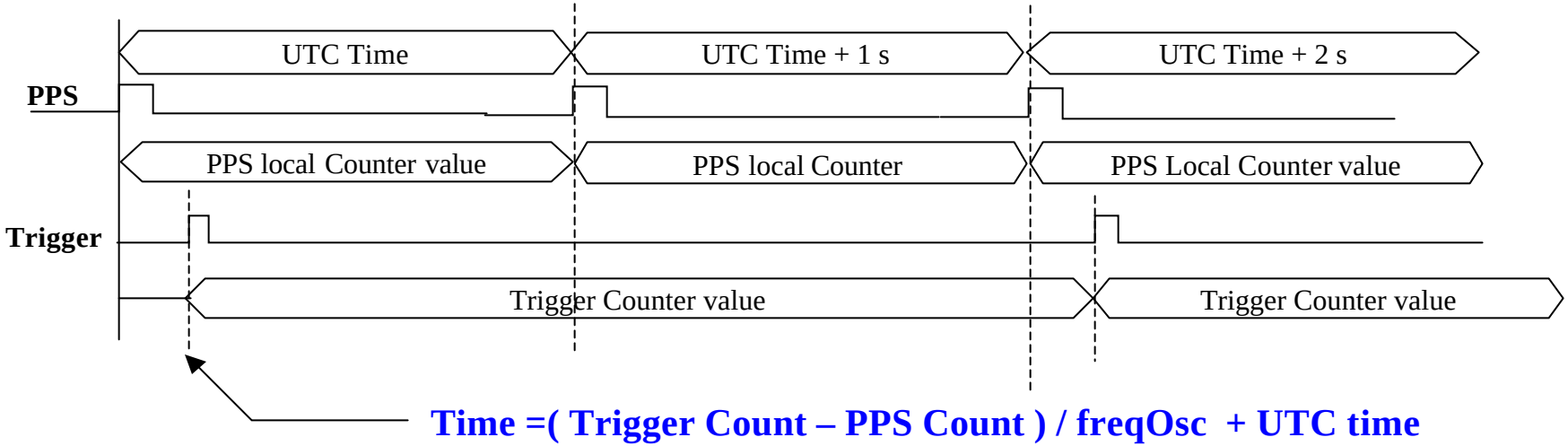
Data streaming application



- Special function for continuous data acquisition.
- No longer use of http command
- With the BFOOT **1 Mbps** of data can be achieved

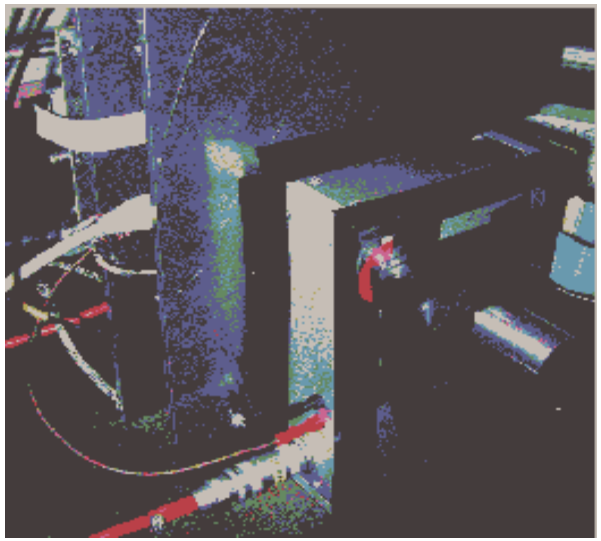
Time stamping

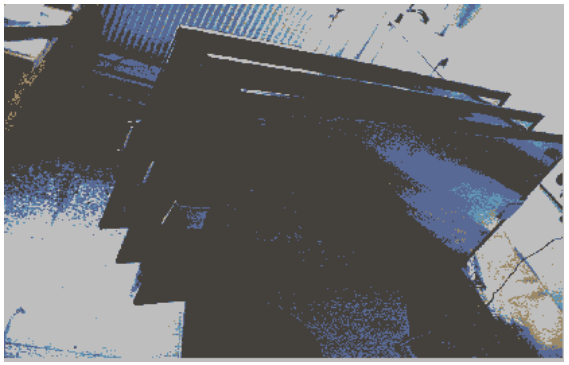




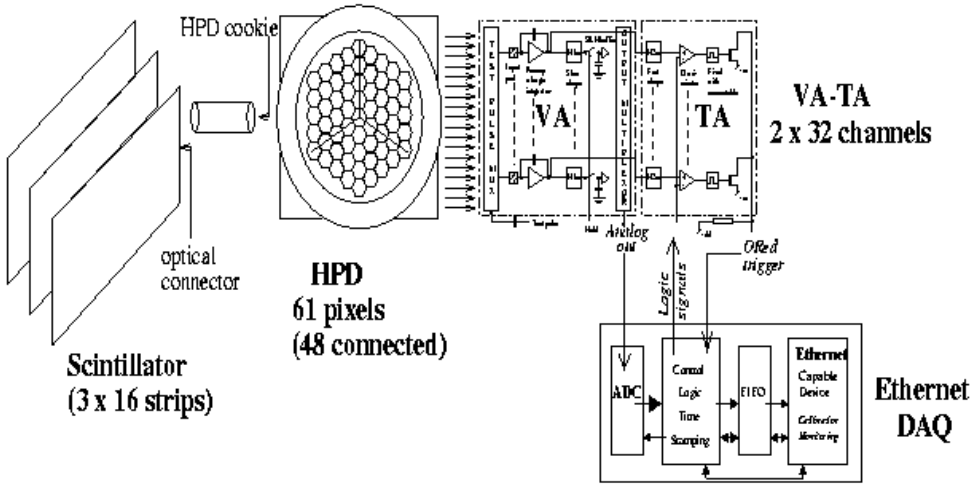
Time =(Trigger Count – PPS Count) / freqOsc + UTC time

(An accumulation of the local counter value over a few seconds can provide a mean value for freqOsc)
ASCII UTC distriuted at start of run, and then updated at each PPS locally





- Tests de Mai-Juin en conditions faisceau
  - 1 Mbit/s obtenu
- Facilite d 'installation:
  - la carte + 1 PC
- Peu de câbles:
  - 1 pour alim +1 ethernet pour les données



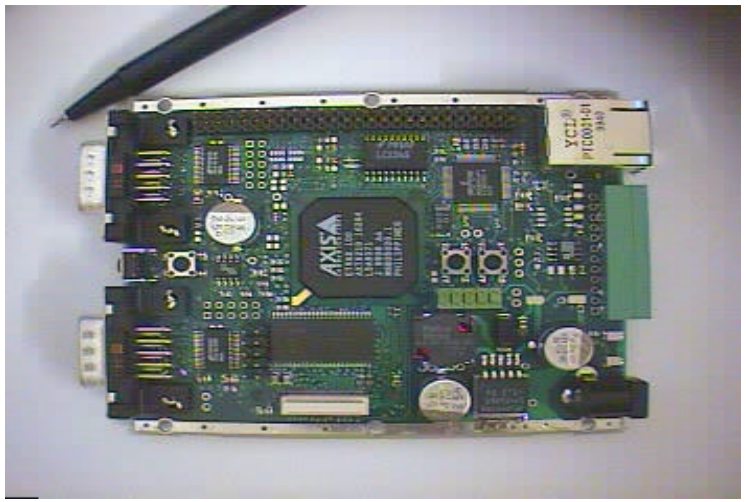
- **Low data rate experiment (100 Hz / channel, 72 kchannels, 96bits/hit)**
- **Aggregate rate 192 Mbit/s/supermodule allows:**
  - **Triggerless mode**
  - **Ethernet for data transmission and event building**
- **Readout can follow modularity of construction (64-128 channels)**
  - **Autonomy, ease of calibration, local intelligence (smart sensor)**
  - **Ethernet visibility: transparency for slow-control and monitoring**
  - **Ethernet « jusqu 'au bout des ongles »**
- **Use industrial solutions (Ethernet, PC 's, Java?)**
- **Embedded Ethernet/Java in full industrial expansion (cellular phones, smart houses,…) drives the costs low (10-30/chip)**

Status and Future on Ethernet DAQ

➢ **Readout of HPD / PMT auto-triggerable F.E.**

❑ Chip compatibility :

- VArich - TA32cg (HPD/APD) ok
- VAhdr11 - TA32cg *(minor changes) (MaPMT)*
- **All Viking chips are in principle readable**



➢ **Future tests & developments** :

New Ethernet controller (ETRAXS)
100 Mbits/s, low power,
embedded Linux ,35$

❑ Design of a compact Ethernet F.E. module +analog FE

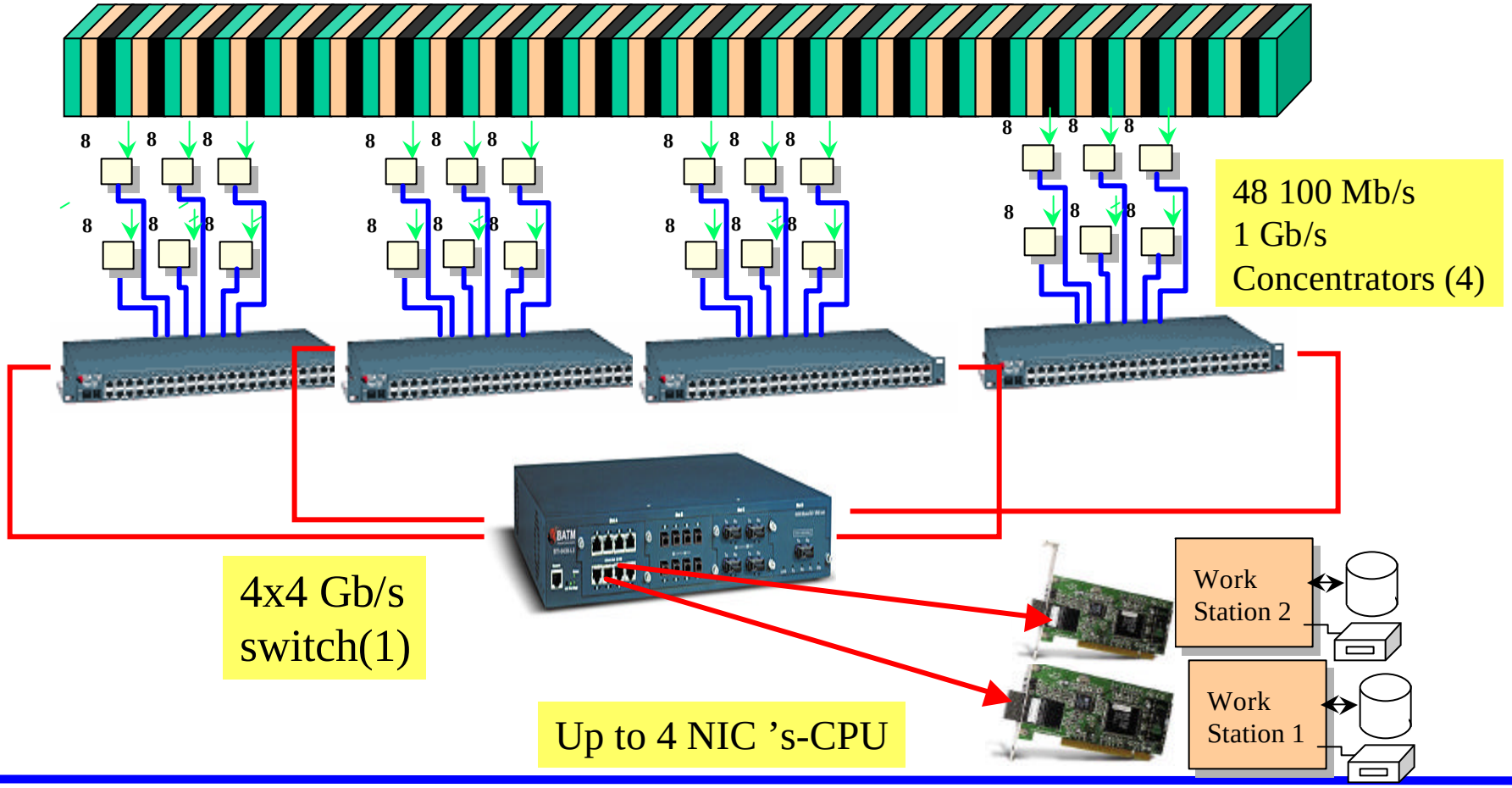
❑ Possibility to make a series? e-TDC, e-ADC,e-DAC ?

❑ Possibility to for compact e-PMT modules?

❑**Test of event-building (~500 Ethernet nodes) in collaboration with the group of simulation of ATLAS HLT (K. Krorcyl, P. Golonka R. Dobinson et al)**

Proposal of an acquisition scheme

SuperModule 1=24 X/Y biplanes =192 nodes = 384 64 channel FE 's

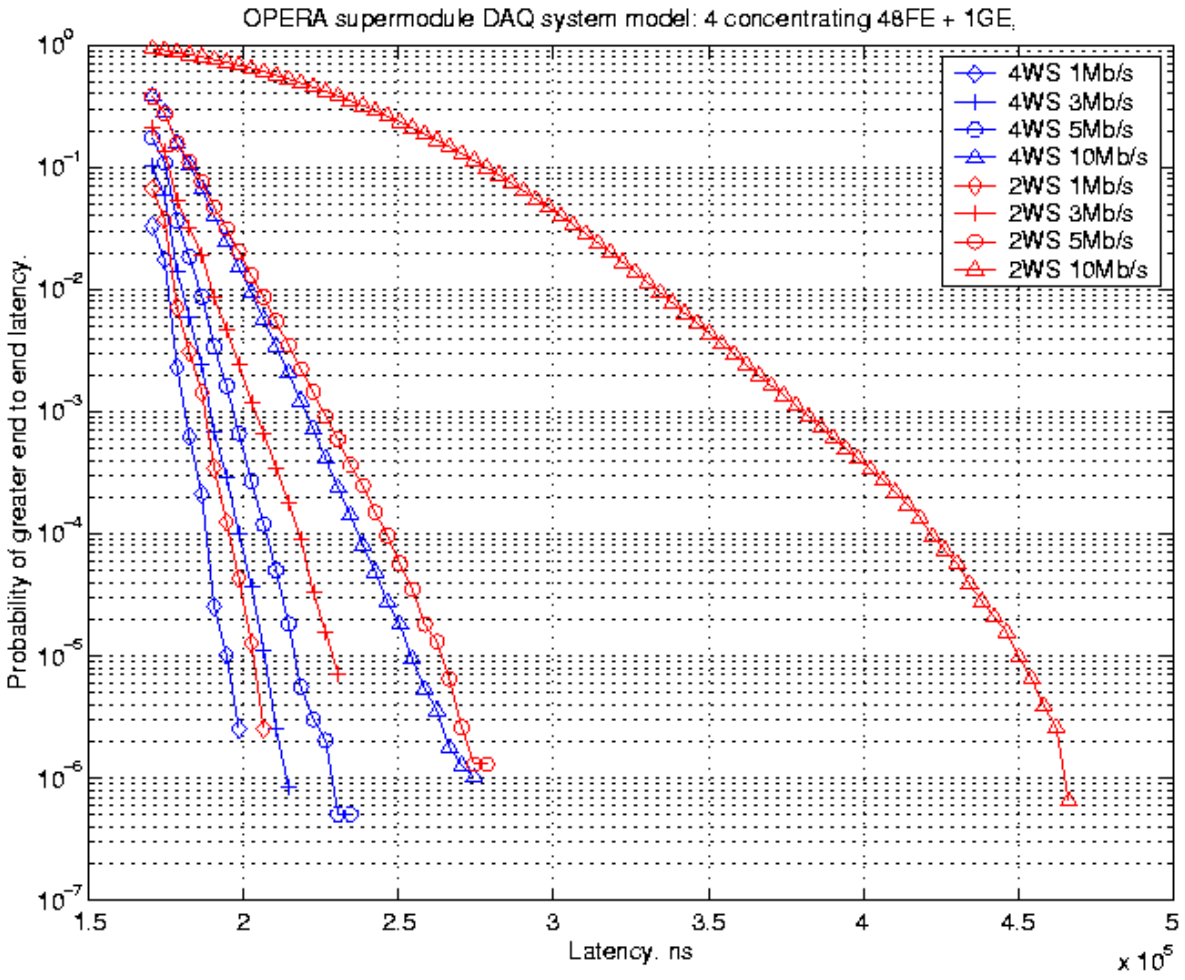


Une possibilité d ’occuper utilement la bande passante

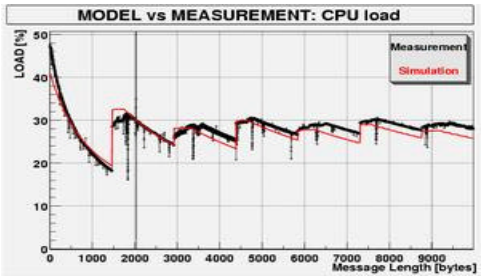
	concentrating switch				workstation			
	1	2	3	4	1	2	3	4
1 second:	1				0.25(1)			
2 second:	2	1			0.50(1)	0.25(2)		
3 second:	3	2	1		0.75(1)	0.50(2)	0.25(3)	
4 second:	4	3	2	1	1.00(1)	0.75(2)	0.50(3)	0.25(4)
5 second:	5	4	3	2	0.25(5)	1.00(2)	0.75(3)	0.50(4)
6 second:	6	5	4	3	0.50(5)	0.25(6)	1.00(3)	0.75(4)
7 second:	7	6	5	4	0.75(5)	0.50(6)	0.25(7)	1.00(4)
8 second:	8	7	6	5	1.00(5)	0.75(6)	0.50(7)	0.25(8)
9 second:	9	8	7	6	0.25(9)	1.00(6)	0.75(7)	0.50(8)

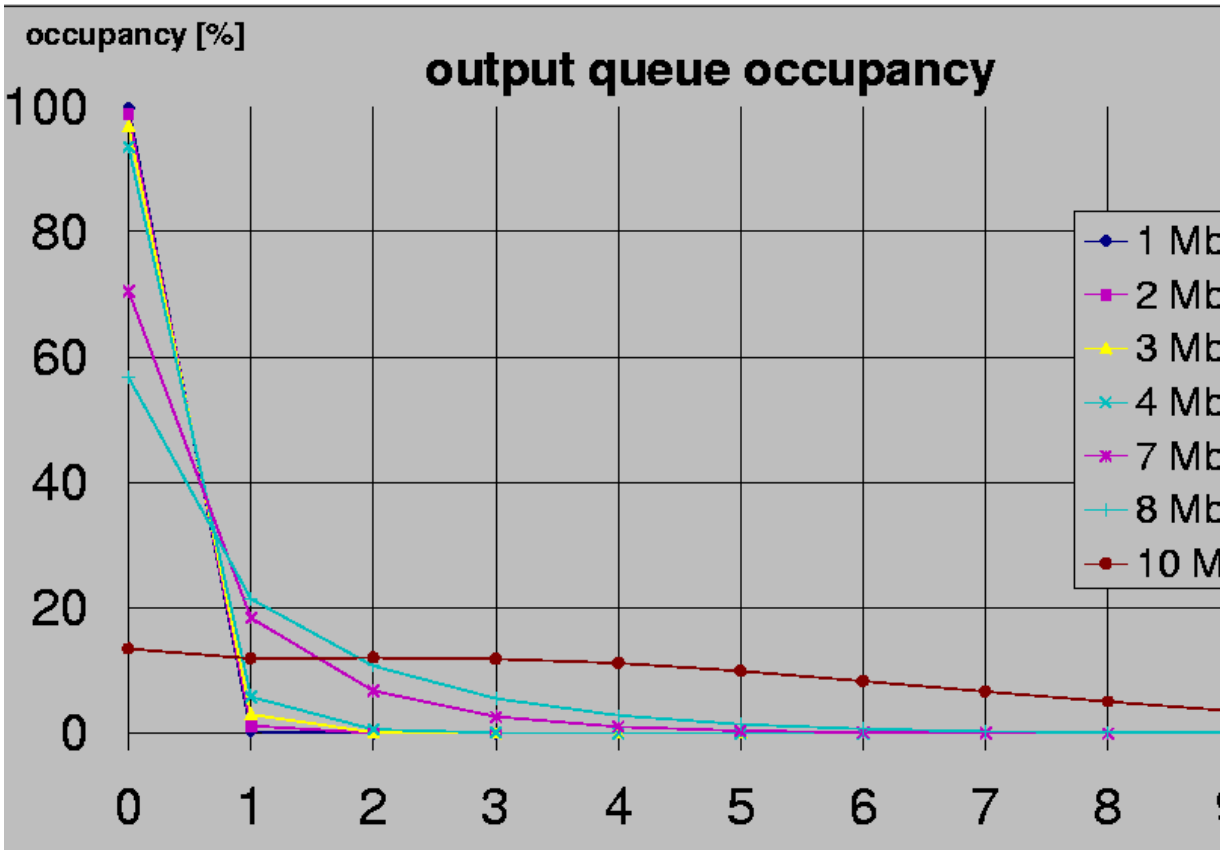
- On est loin de la congestion et les transitions de phase avec les débits existants

- Groupe ATLAS Simulation (PTOLEMY) des switches commerciaux (BATM) complète, testée avec le hardware.



- Scalabilité des processus?
  - Select() impossible
  - SIGIO 20-25\% de la CPU
- TCP/IP complet en Octobre, et estimation (calibrée) d ’occupation de la CPU



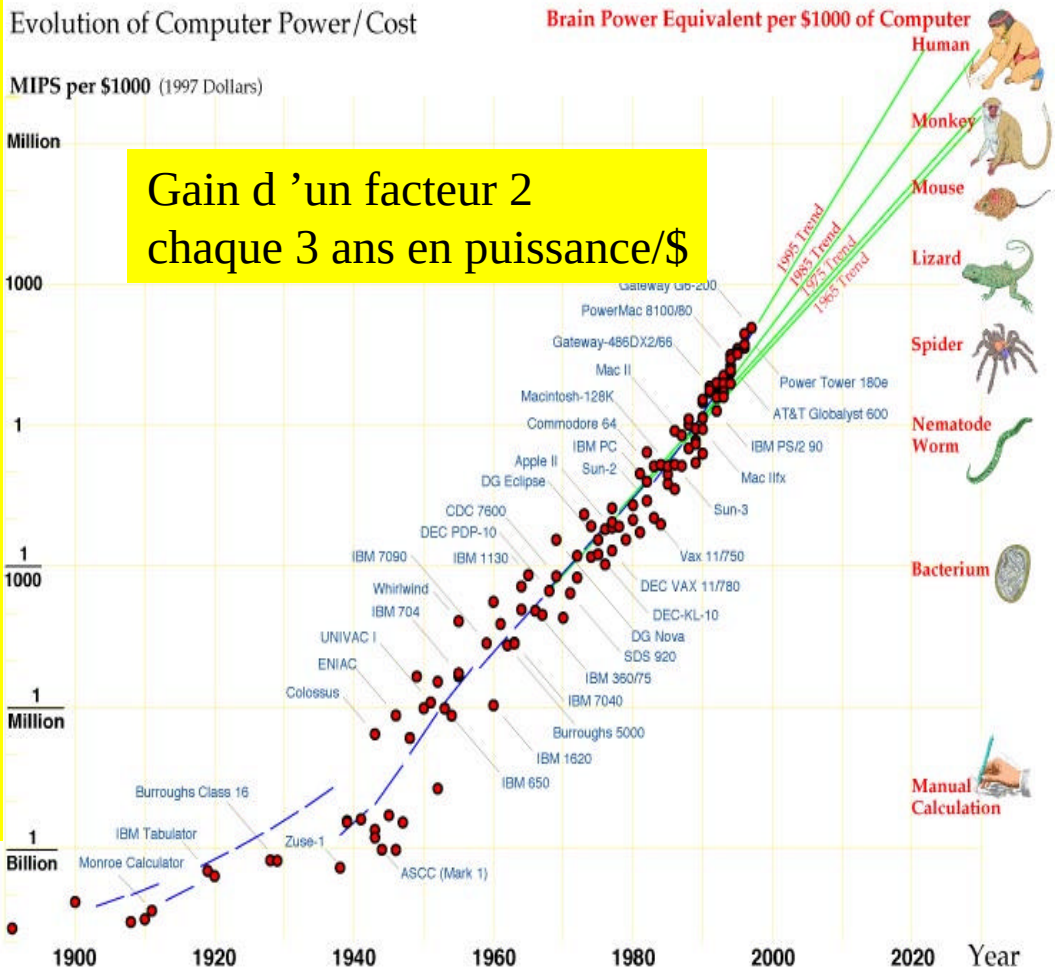


Conclusions et Perspectives

- Un premier prototype de capteur intelligent avec un ADC 25 MHz(+DAC pour ajuster des biais) a été construit et testé en condition faisceau.
- Le processeur ETHERNET utilisé a donné pleine satisfaction, malheureusement HP a décidé d'arrêter sa production
  - *On a commencé des tests avec un nouveau chip LINUX le ETRAX . LINUX = moins de risque*
- On a commencé la modélisation du réseau avec le groupe trigger ATLAS-simulation,
  - *Premiers résultats satisfaisants*
  - *Simulation TCP/IP complète en Octobre*
- **L'idée des capteurs intelligents Ethernet a un grand avenir devant elle**
  - *On est prêt a collaborer pour d 'autres projets, et/ou valider ces idées en industrie*

Le guide du Routard de l'online :

- Amener les données au plus vite vers une plage CPU
- Ne pas rester chez soi et écrire des codes ésotériques pour des machines ésotériques
- Eviter de prendre le bus (même pas PCI)
- Sortir directement a l 'autoroute Ethernet 1Gb/s--> 10 Gbit/s-->?
- Eviter les embouteillages (congestion) avec des bons commutateurs



Gain d 'un facteur 2 chaque 3 ans en puissance/$

Plus adaptée pour astroparticules que l 'LHC mais voir ATLAS/CMS HLT