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PARISROC, a Photomultiplier Array Integrated Readout Chip.

Selma Conforti Di Lorenzo[a], J. E Campagne[a], Christophe De La Taille[a], Sebastien Drouet[b], Dominique Duchesneau[c], Frederic Dulucq[a], Nicolas Dumon-Dayot[c], Abdelmowafak El Berni[a], Alexandre Gallas[a], Bernard Genolini[b], Kael Hanson[d], Richard Hermel[c], Gisele Martin-Chassard[a], T. Nguyen Trung[b], Jean Peyré[b], Joël Pouthas[b], Emmanuel Rindel[b], Philippe Rosier[b], Jean Tassan Viol[c], Eric Wanlin[b], Wei Wei[e], Xiongbo Yan[e], Beng Yun Ki[b], A. Zghiche[c].

[a] *Laboratoire de l'Accélérateur Linéaire,IN2P3-CNRS, Université Paris-Sud 11, Bât. 200, 91898 Orsay Cedex, France*
[b] *Institut de Physique Nucléaire d'Orsay, IN2P3-CNRS, Université Paris-Sud, 91406 Orsay Cedex, France*
[c] *Laboratoire d'Annecy-le-vieux de Physique des Particules IN2P3-CNRS,Université de Haute Savoie*
[d] *Université Libre de Bruxelles, Université d'Europe Bruxelles*
[e] *IHEP, Beijing, China*

E-mail: conforti@lal.in2p3.fr

ABSTRACT: PARISROC is a complete read out chip, in AMS SiGe 0.35 μm technology [1] , for photomultipliers array. It allows triggerless acquisition for next generation neutrino experiments and it belongs to an R&D program funded by French national agency for research (ANR) called PMm2: "'Innovative electronics for photodetectors array used in High Energy Physics and Astroparticles"' [2] (ref.ANR-06-BLAN-0186). The ASIC integrates 16 independent and auto triggered channels with variable gain and provides charge and time measurement by a 12-bit ADC and a 24-bit Counter. The charge measurement should be performed from 1 up to 300 pe with a good linearity. The time measurement allowed to a coarse time with a 24-bit counter at 10 MHz and a fine time on a 100ns ramp to achieve a resolution of 1 ns. The ASIC sends out only the relevant data through network cables to the central data storage.

KEYWORDS: Keyword1; Keyword2; Keyword3.

Contents

1. Introduction

The PMm2 project: "'Innovative electronics for photodetectors array used in High Energy Physics and Astroparticles"' [2] proposes to segment the large surface of photodetection in macro pixel consisting of an array of 16 photomultipliers connected to an autonomous front-end electronics (Fig. 1) and powered by a common High Voltage. These large detectors are used in next generation proton decay and neutrino experiment (i.e. the post-SuperKamiokande detectors as those that will take place in megaton size water tanks) and will require very large surfaces of photo detection and a large volume of data. The micro-electronics group's (OMEGA from the LAL at Orsay) purpose is the front-end electronics conception and realization. This R&D [2] involves three French laboratories (LAL Orsay, LAPP Annecy, IPN Orsay) and ULB Bruxells for the DAQ. It is funded for three years by the French National Agency for Research (ANR) under the reference ANR-06-BLAN-0186.

LAL Orsay is in charge of the design and tests of the readout chip named PARISROC which stands for Photomultiplier ARrray Integrated in Si-Ge Read Out Chip.

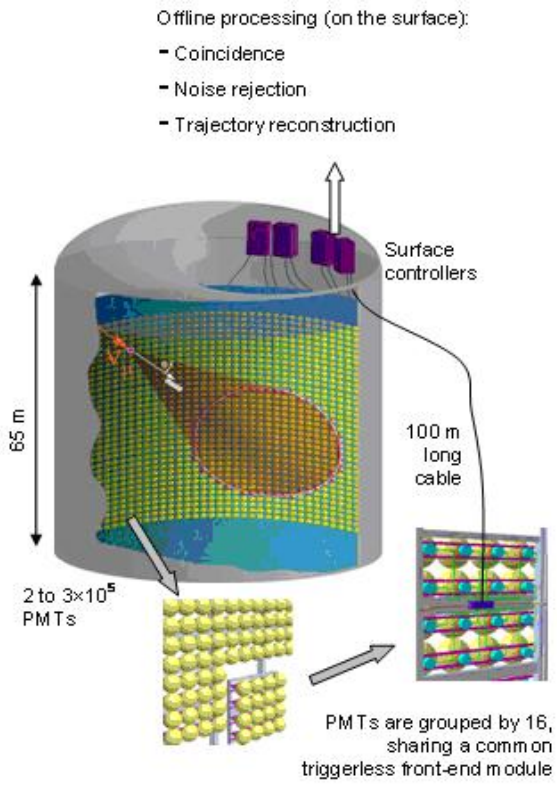

Figure 1. Principal of PMm2 proposal for megaton scale Cerenkov water tank.

The detectors such as SuperKamiokande, are large tanks covered by a significant number of large photomultipliers (20"), the next generation neutrino experiments will require a bigger surface of photo detection and thus more photomultipliers. As a consequence the total cost has an important relief [1]. The project proposes to use 12" PMts with an improved cost (by factor of 1.6 in comparison to 20 ") per unit of surface area and detected p.e (cost/QE*CE). This is mainly due to the different industrial fabrication of the PMTs, the better photon detection efficiency and a better reliability. The reduced costs are, also, due to:

- A smaller number of electronics, thanks to the 16 PMTs macropixel with a common electronics, even if it induces more electronic channels;
- A common High Voltage for the 16 PMTs so a reduced number of underwater cables, cables that are also used to brought the DATA to the surface;
- The front-end closed to the PMTs that allow a suppression of underwater connector.

The general principle of PMm2 project is that the ASIC and a FPGA manage the dialog between the PMTs and the surface controller (Fig. 2). Alternative options may be chosen considering an analysis of the risks of this full underwater strategy,one of these is that the Front-End electronics can be used in a traditional schema with the electronic "in surface". PARISROC can be perfectly integrated in a surface scheme.

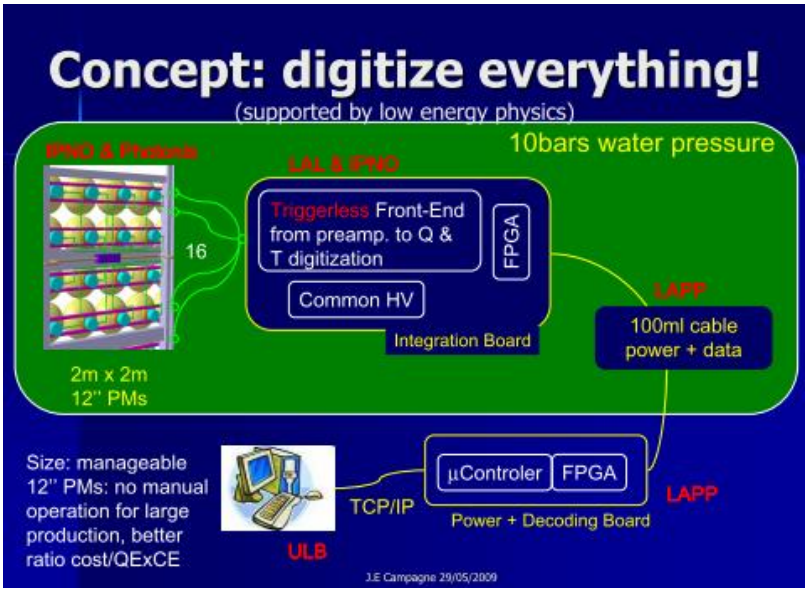

Figure 2. Principle of the PMm2 project.

2. PARISROC architecture

2.1 Requirements

The physics events, researched in this detectors, produce Cerenkov light that is spread over the PMTs. The number of events in this kind of experiences is "rare" and the number of pe per Mev deposed in the water is of 10pe/MeV on one circular scheme over 10000 PMTs. So for few MeV events the small number of p.e is spread over a large number of PMTs and as consequence is necessary being fully efficient to detect a single photo-electron (p.e). For large energy events (such as supernova events) it is shown, in Superkamiokande experiment, that the dynamic range for a single PM should cover up to few hundred p.e (300pe). All the type of events considered must be registered without any direct external trigger, this later is called 'triggerless mode'. A precise time stamp of each event is required to reconstruct the topology of the events and so to synchronize the events among PMTs in each array and among the different arrays. This aspect brought to an requirement: an electronic with full independent channels. The most demanding in term of timing is the vertex reconstruction that needs typically 1 ns resolution. The pe, reached by the PMTs, are multiplied with a gain G of 3*106; this value is owed to a cost reason. The array of PMTs is not homogeneous in terms of gain because of the common HV. A better homogeneity should have brought to an increasing of the costs. It was estimate from a study that the gain dispersion at a given voltage is such that the ratio between the highest and the lowest gain is not more than 12. It is possible for the manufacturer to sort the PMTs at a reasonable cost when they are produced at a very large scale: the gain ratio can be reduced ton 6 in a batch of 16 PMTs. To compensate this not homogeneity a preamplifier with a variable and adjustable gain is required (structure explain in the next section. Finally the electronic requirements must be:

- 1pe of efficiency

- triggerless
- 1ns of time resolution
- high granularity
- scalability
- low cost
- independent channels
- charge and time measurement
- water-tight, common High Voltage
- only one wire out (DATA + VCC)

2.2 Analogue Channel description and simulations

The ASIC Parisroc is composed of 16 analogue channels managed by a common digital part (Fig. 3).

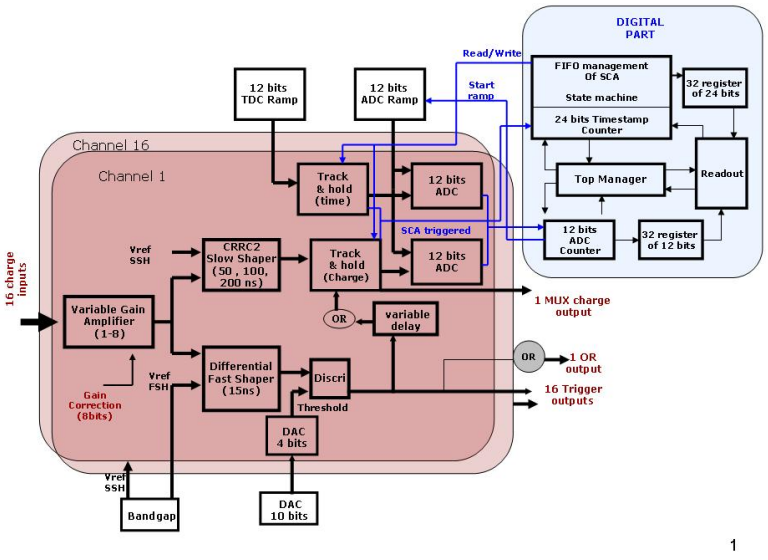

Figure 3. PARISROC global schematic.

Each analog channel is made of a low noise preamplifier with variable and adjustable gain. The variable gain is common for all channels and it can change on 4 bits thanks to the input variable capacitance (Cin from 1 to 4 pF). The gain is also tuneable channel by channel, to adjust the input detector not homogeneous gains, on 8 bit thanks to a feedback variable capacitance (Cf from 1 to 0.007pF with step of 1/2). The gain (G=Cin/Cf) can be adjustable on 8 bit for each channel. The preamplifier is followed by a slow channel for the charge measurement in parallel with a fast channel for the trigger output.

The slow channel is made by a slow shaper followed by an analogue memory with a depth of 2 to provide a linear charge measurement up to 50 pC; this charge is converted by a 12-bits Wilkinson ADC. One follower OTA is added to deliver an analogue multiplexed charge measurement.

The fast channel consists in a fast shaper (15 ns) followed by 2 low offset discriminators to auto-trig down to 50 fC. The thresholds are loaded by 2 internal 10-bit DACs common for the 16 channels and an individual 4bit DAC for one discriminator. The 2 discriminator outputs are multiplexed to provide only 16 trigger outputs. Each output trigger is latched to hold the state of the response until the end of the clock cycle. It is also delayed to open the hold switch at the maximum of the slow shaper. An "'OR"' of the 16 trigger gives a 17th output.

For each channel, a fine time measurement is made by an analogue memory with depth of 2 which samples a 12-bit ramp, common for all channels, at the same time of the charge. This time is then converted by a 12 bit Wilkinson ADC.

The two ADC discriminators have a common ramp, of 8/10/12 bits, as threshold to convert the charge and the fine time. In addition a bandgap bloc provides all voltage references.

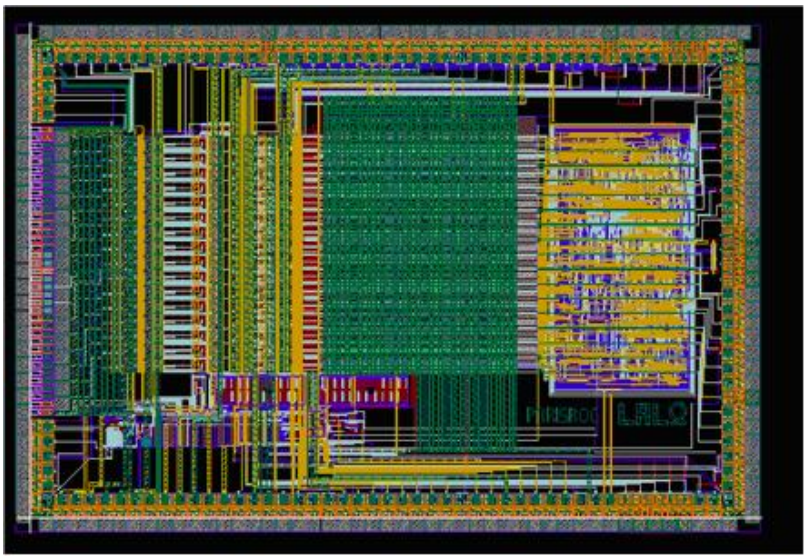

Figure 4. PARISROC Layout.

Fig. 5 represents, in a schematic way, the detail of one channel analogue part.

2.3 Preamplifier

The input preamplifier is a low noise preamplifier with variable gain thanks to the switched input (C_{in}) and feedback (C_f) capacitors that can be adjusted (Fig. 6).

This gain can vary changing C_{in}, which is common to the 16 channels, over 4 bits and C_f, to adjust preamplifier gain channel by channel. This adjustment allows correction of the PMT gain dispersion due to a use of a common HV.

The preamplifier is designed as a voltage preamplifier in p-type Cascode structure to allow the acquisition of a fast input signal with a large dynamic range.

The input transistor is a PMOS in common source configuration: $W = 800\ \mu$m; $L = 0.35\ \mu$m; the big input transistor is chosen to keep the preamplifier noise contribution low and to achieve

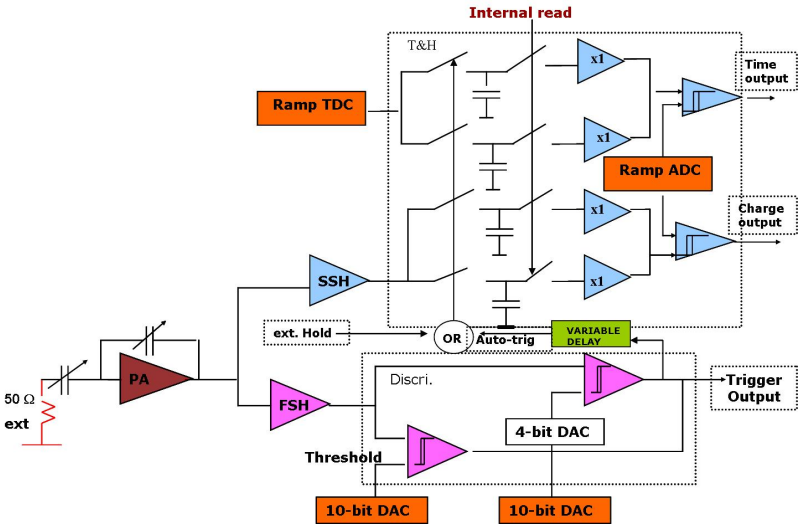

Figure 5. PARISROC one channel analogue part schematic.

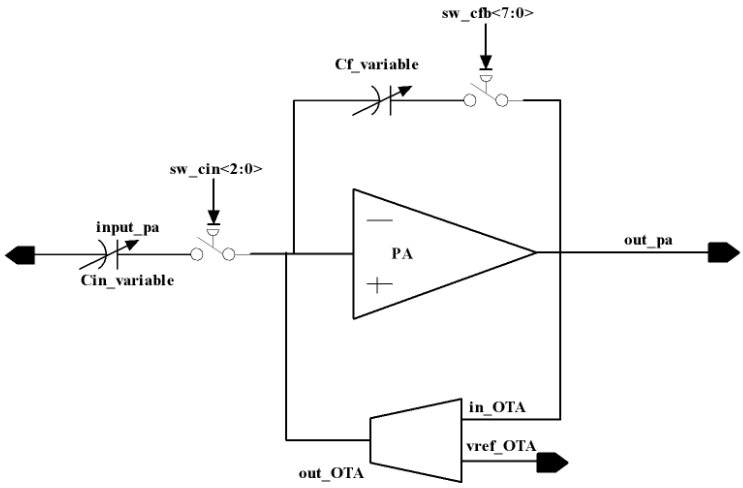

Figure 6. PARISROC preamplifier schematic.

a high gm. It supplies the output (the drain terminal) to the input terminal (source terminal) of the second stage transistor: $W = 100$ μm; $L = 0.35$ μm; the output transistor must be small to reach preamplifier high speed performances. The utility of the cascode preamplifier is in the large input impedance of the common source (with also the characteristic of Current Buffer) and better frequency response of a common Gate. An output buffer stage is designed in order to adapt the output impedance to the loaded impedance. The input dc level is high (about 2.6 V) while the output dc level is low (about 1 V). Because of the single side structure of preamplifier, it is hard to use the external reference voltage to set the dc operating point; the idea is to use an OTA as the dc feedback amplifier.

In Fig. 7 are shown preamplifier's output waveforms for fixed gain and different input signal (left panel) and for fixed input signal and different preamplifier gain (right panel).

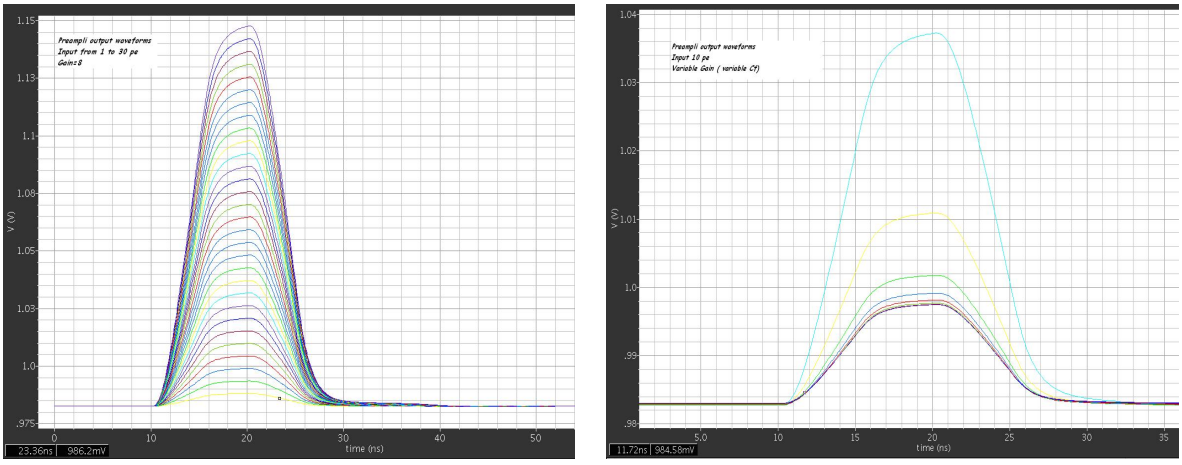

Figure 7. Simulated preamplifier output waveforms for different input signals with fixed gain (left panel) and for fixed input signal at different gain (different input capacitor values (right panel).

Table 1. TO BE COMPLETED

G_{pa}	$V_{out-max}$	Qi_{max}/n_{pe}	Residuals (%)
8	1.394 V	40 pC/250 pe	-0.6 to 0.2
4	0.841 V	48 pC/300 pe	-0.1 to 0.3
2	0.417 V	48 pC/300 pe	-0.2 to 0.3

The input signal, used in simulation, is a triangle signal with 4.5 ns rise and fall time and 5 ns of duration as shown in Fig. 8. This current signal is sent to an external resistor (50 Ohms) and varies from 0 to 5 mA in order to simulate a PMT charge from 0 to 50 pC which represents 0 to 300 photo-electrons when the PM gain is 10^6.

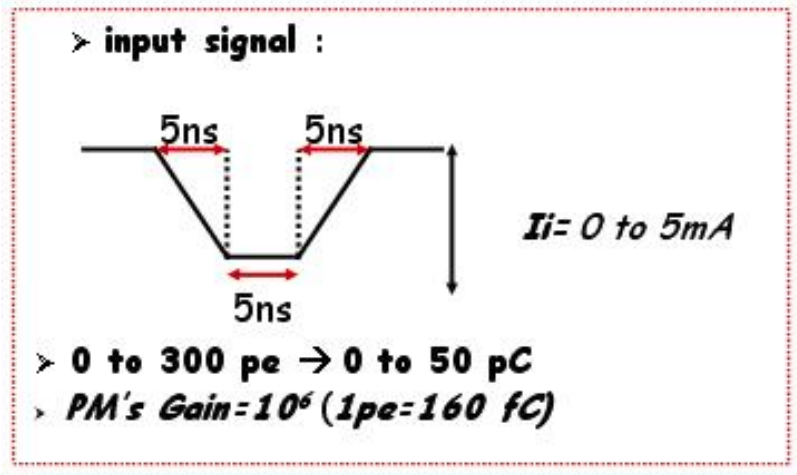

Figure 8. Simulation input signal.

The Fig. 9 displays the input dynamic range allowed to the preamplifier linearity performance. Tab. 1 lists the residuals obtained for different gains and shows a good linearity (better than $\pm 1\%$).

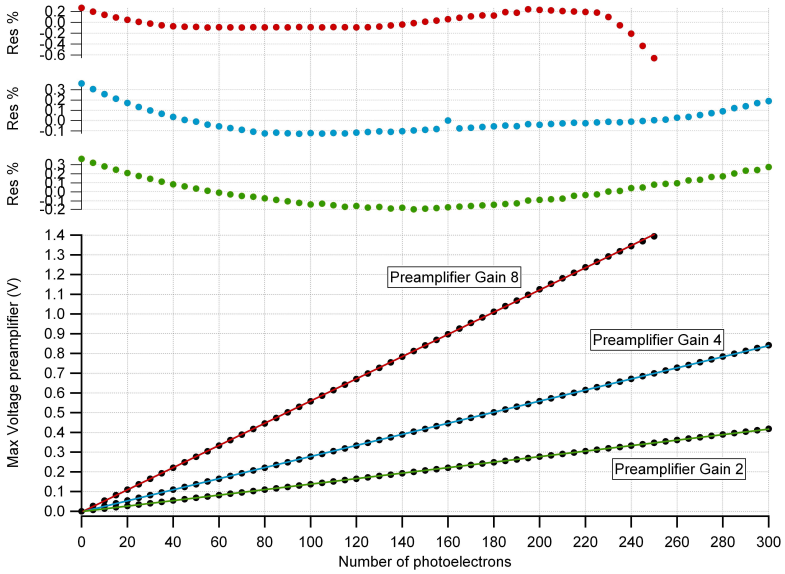

Figure 9. Preamplifier linearity.

Table 2. TO BE COMPLETED

RMS	SNR	$V_{out}(1p.e)$
468 μV ($\approx 1/12$ p.e, $\approx$ 13 fC)	11.6	5.43 mV

The Fig. 10 displays the preamplifier noise with an rms value of 13 fC and a Signal to Noise ratio of $\approx$ 12. Tab. 2 summarizes the results obtained.

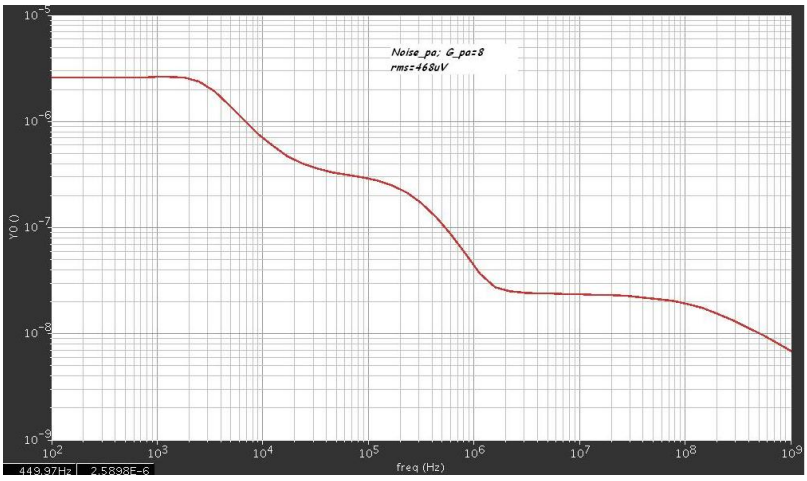

Figure 10. Preamplifier noise simulation; $G_{pa} = 8$; $C_{in} = 4$ pF and $C_f = 0.5$ pF.

2.4 Trigger output

The PARISROC is a self-triggered device. The fast channel has been conceived for this purpose.The amplified signal flows in a fast shaper that is a CRRC filter with a time constant of

Table 3. To be completed

RMS	SNR	$V_{out}(1p.e)$	T_p
2.36 μV ($\approx 1/16$ p.e, ≈ 10 fC)	16	37.85 mV	8 ns

15 ns. Its high gain allows to send high signal to the discriminator and thus to trigger easily on 1/3 of photo-electron. It has a classical design: differential pair is followed by a buffer.

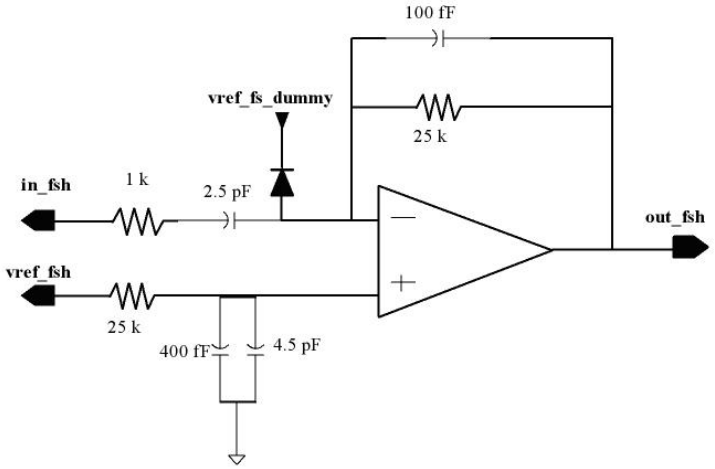

Figure 11. Fast shaper schematics.

The Fig. 12 represents the fast shaper output waveforms for a variable input signal. The Tab. 3 lists the fast shaper principal characteristics obtained in simulation.

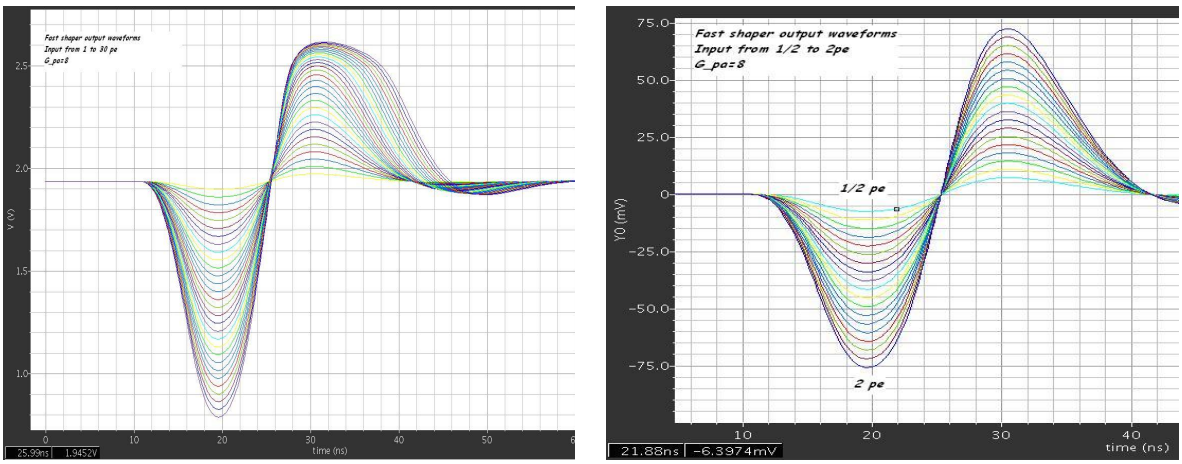

Figure 12. Simulated fast shaper outputs ($G_{pa} = 8$ with input from 1-10 pe (left panel) and from 1/3 pe to 2 pe (right panel).

The fast shaper (15 ns) is followed by a low offset discriminator to auto-trig down to 50 fC (1/3 pe at 10^6 gain).

The two discriminators can be used alone or simultaneously. Their outputs are multiplexed to ease the choice. Both are simple low offset comparators with the same schematic. The difference comes from the way to set the threshold. The first discriminator has the threshold sets by one 10-bit DAC, common to all 16 channels, and one 4-bit DAC for each channel. The second discriminator has the threshold sets by only the 10 bit common DAC. Each output trigger is latched to hold the state of the response in SCA channel. In Fig. 13 are shown the triggers and the zoom of the triggers rise time in order to see the time walk of around 4 ns.

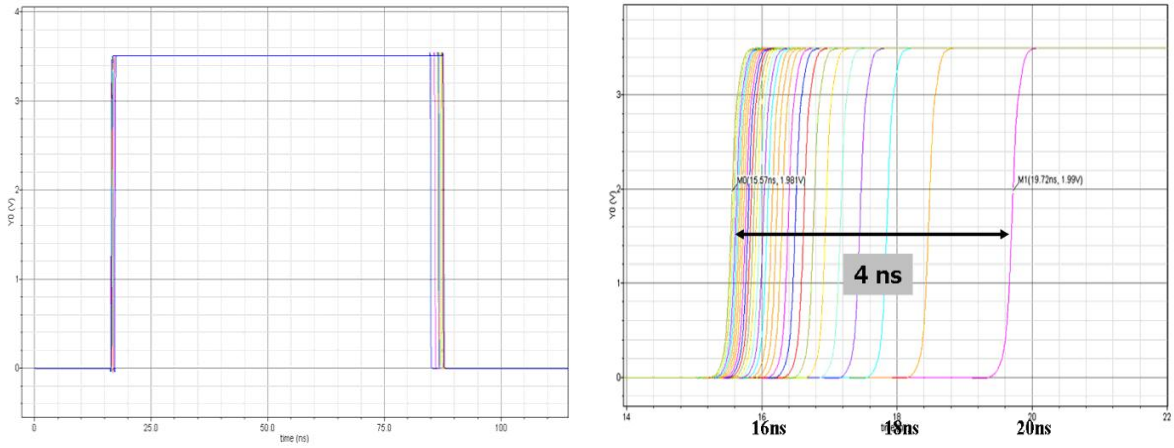

Figure 13. Simulated trigger output (input charge from 0 to 10 p.e; threshold at 1/3 p.e). Zoom of trigger rise time on right pannel.

Each output trigger is latched to hold the state of the response in SCA channel. SCA channel is the also called "'Analogue memory"'. The SCA has a depth equal to two; this means that there are two T&H for time measurement as well as for charge measurement.

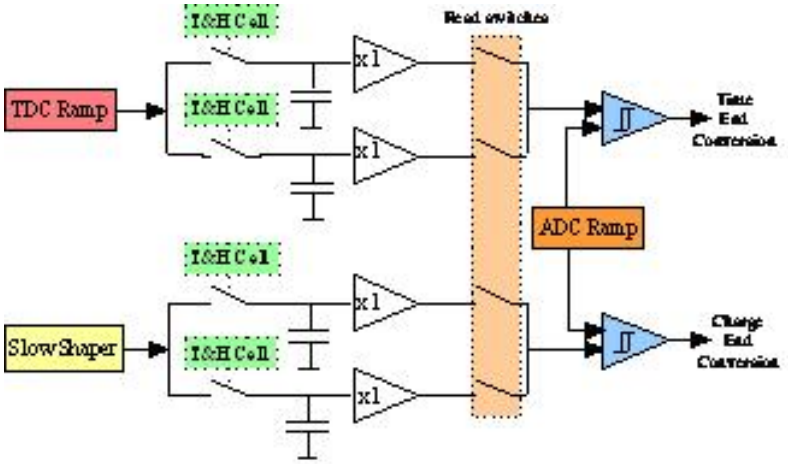

Figure 14. SCA (switched capacitor array) scheme.

The voltage level of the signal coming from slow shaper or ramp TDC cell is memorised in the T&H capacitor (500 fF) so "'Track & Hold Cell"' allows to lock the capacitor value only when

a calibrated trigger (from fast channel) occurs within the selected column. The SCA column is selected, read and erased by the digital part.

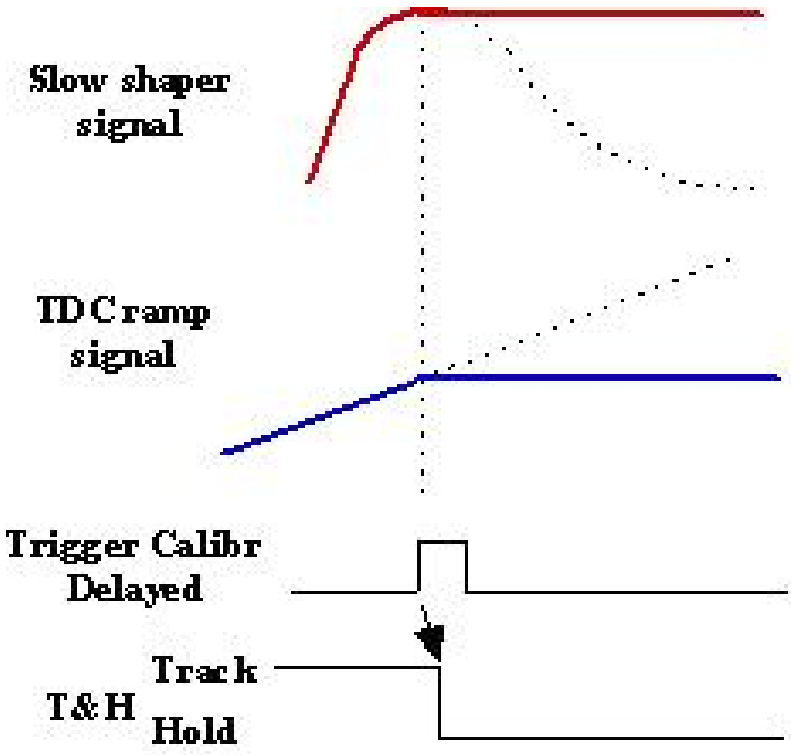

Figure 15. Operation of T&H cell.

On Fig. 15 is illustrated the T&H cell mode of operation: when a signal arrives in the discriminator cell is detected and the output trigger signal is sent to the T&H cell. The output trigger is delayed and calibrated before being sent.

2.5 Charge channel

The charge channel is the slow channel: the signal amplified by the variable gain preamplifier is sent to the slow shaper, a typical CRRC^2 filter with variable peaking time. The peaking time can be set from 50 ns (default value) to 200 ns thanks to the switched feedback capacitors.

On left part of Fig. 16 are represented the slow shaper waveforms for different shaping times and the same input signal. The noise value (Tab. 4 and right part of Fig. 16), from 980 μV to 1.6 mV (simulation results), foresee good noise performance.

The Fig. 17 and Tab. 5 illustrate the linearity performance for different time constants. Simulations show a good linearity with residuals from -0.5% to 0.2% at $T_p = 50$ ns, from -1% to 0.3% at $T_p = 100$ ns and -0.7% to 0.3% at $T_p = 200$ ns.

The Slow shaper maximum value, therefore the charge value, is then memorized in the analogue memory, with a depth of 2, thanks to the delayed trigger. Fig. 18 gives the simulated slow shaper and SCA signals.

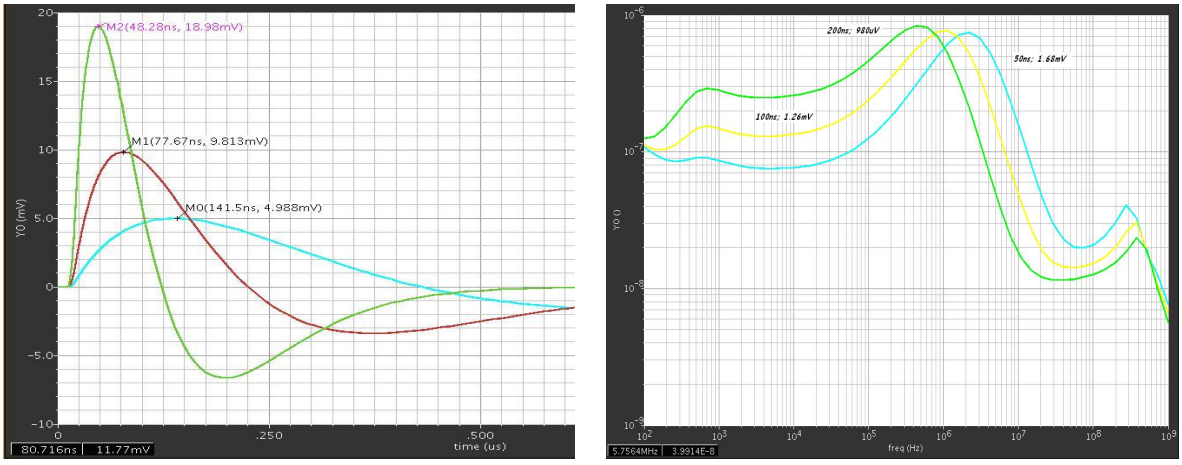

Figure 16. Slow shaper output waveforms simulation (left panel). Slow shaper output noise simulation (right panel).

Table 4. TO BE COMPLETED. $G_{pa} = 8$

Time constant	RMS	SNR	$V_{out}(1p.e)$
50 ns	1.68 mV $\approx 1/17$ p.e ≈ 9 fC	11	29 mV $T_p = 48$ ns
100 ns	1.26 mV $\approx 1/12$ p.e ≈ 20 fC	8	15 mV $T_p = 78$ ns
200 ns	0.98 mV $\approx 1/5$ p.e ≈ 32 fC	5	8 mV $T_p = 141.5$ ns

Table 5. TO BE COMPLETED

Time constante	$V_{out-max}$	Qi_{max}/n_{pe}	Residuals (%)
50 ns	1.437 V	13 pC/80 pe	-0.5 to 0.2
100 ns	1.493 V	24 pC/150 pe	-1.0 to 0.3
200 ns	1.385 V	48 pC/300 pe	-0.7 to 0.3

This charge, stored as a voltage value, is then converted in digital value thanks to the 8/10/12 bit Wilkinson ADC.

2.6 Time measurement

For each channel, a fine time measurement is performed by the analogue memory with a depth of 2 which samples a 12 bit ramp (100 ns), common for all channels, at the same time of the charge.

In Fig. 19 is represented the TDC Ramp general schematic. The current, which flows in feedback, charges the capacitance C_f when the switch is off. When the switch is turned off, C_f discharges. Signals `start\_ramp` and `start\_ramp\_b` manage the switches. The rising signal starts the ramp and the falling signal stop the ramp (Fig. 19).

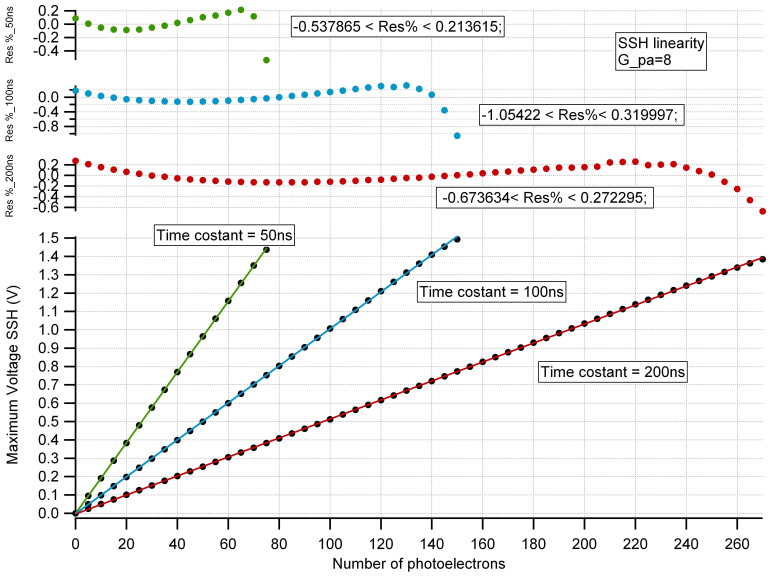

Figure 17. Slow shaper linearity simulation.

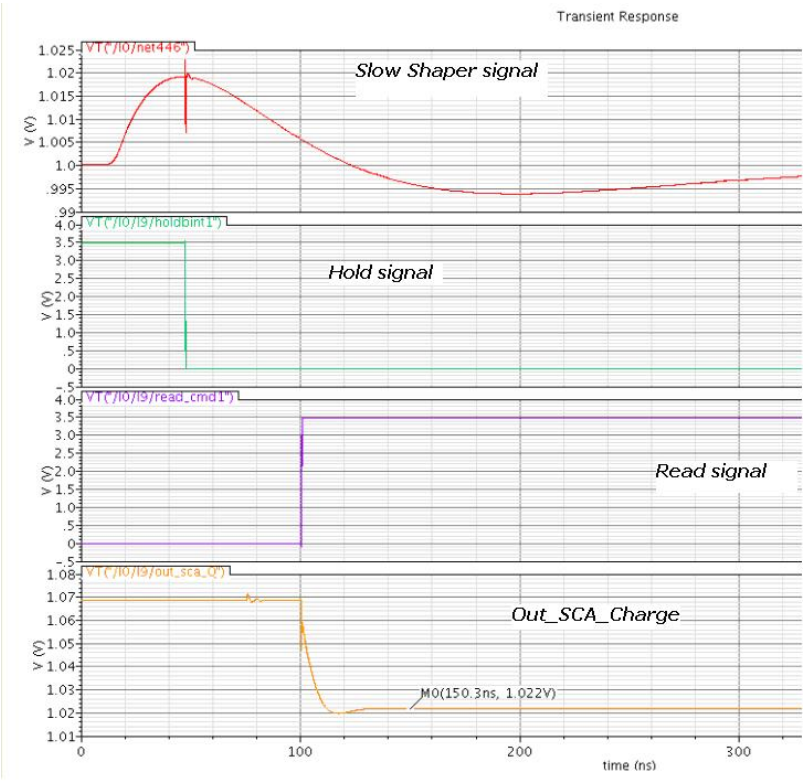

Figure 18. Slow shaper & SCA simulation.

In order to avoid the large falling time of the ramp due to the C_f discharge time and the problem of non linearity at the start and the end of ramp signal (Fig. 20), the real ramp is created from two ramps.

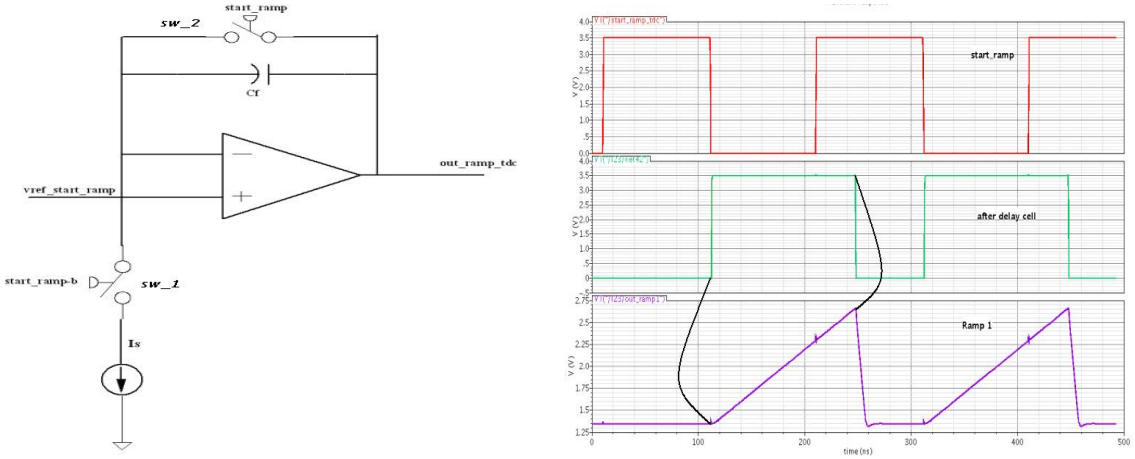

Figure 19. TDC Ramp general schematic.

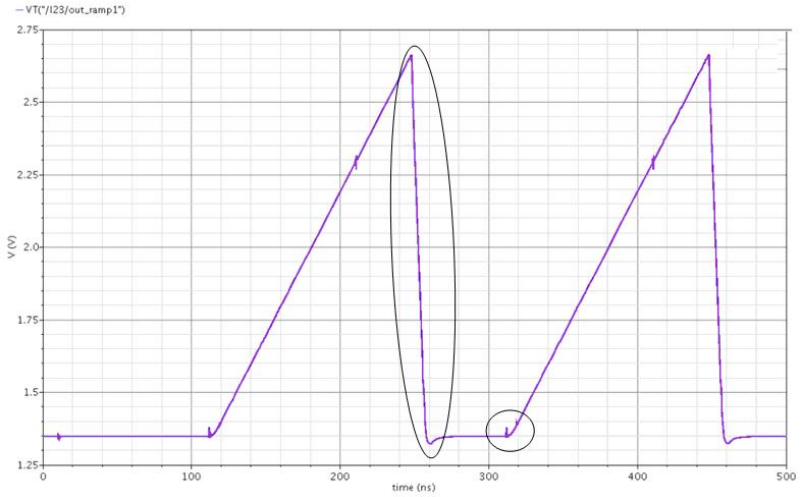

Figure 20. TDC Ramp.

The signal start ramp, coming from the digital part, enters in two delay cells. The two delayed signals create the first and second ramps. Commutating alternatively two switches the 100 ns ramp TDC is created (Fig. 21 and Fig. 22).

This time value, stored as a voltage value, is then converted in digital value tanks to the 8/10/12 bit Wilkinson ADC.

2.7 ADC ramp

In Fig. 23 is represented the Ramp ADC general scheme. It is the same as TDC ramp one, the difference is in a variable current source which allows obtaining 8bit/10bit/12bit ADC according to the injected current. Tab. 6 gives, for each ramp, the time duration to reach 3.3 V.

Then the ADC ramp is compared thanks to a Discriminator to the voltage values, which corresponds to charge and fine time values, stored in the SCA. The digital converted DATA are then treated by the digital part.

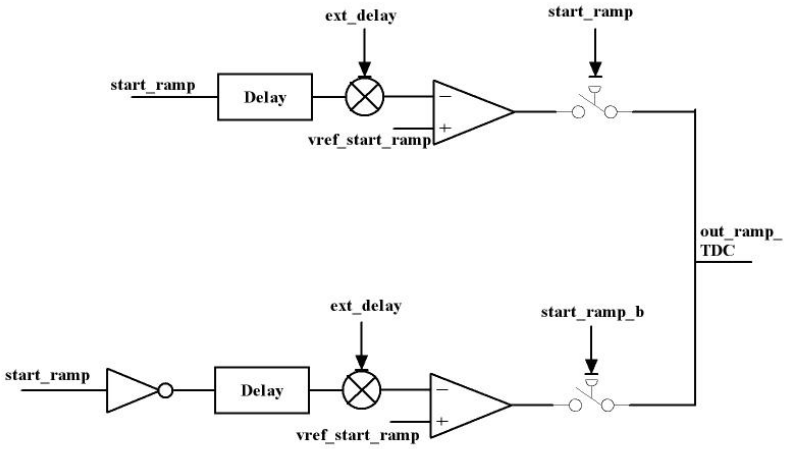

Figure 21. TDC Ramp scheme.

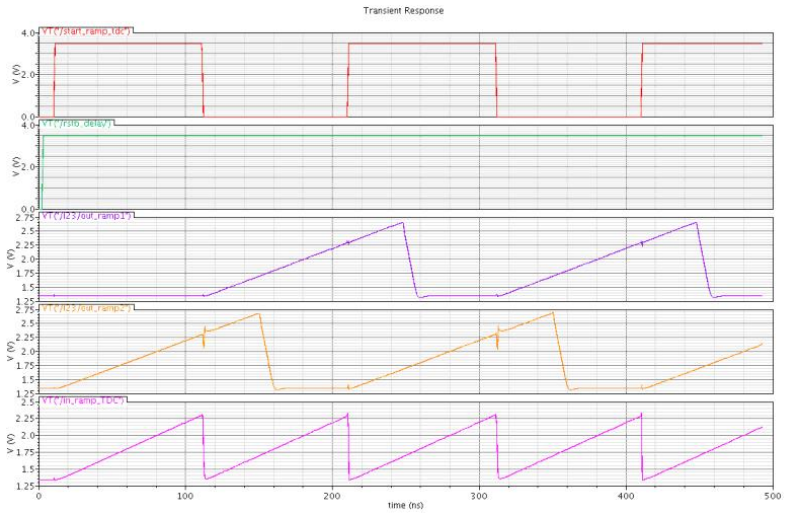

Figure 22. TDC Ramp simulation.

Table 6. TO BE COMPLETED

Header 1	Header 2
12 bit ADC	From 0.9 V to 3.3 V in 102.0 μs
10 bit ADC	From 0.9 V to 3.3 V in 25.6 μs
8 bit ADC	From 0.9 V to 3.3 V in 6.4 μs

2.8 Digital part

The digital part of PARISROC is built around 4 modules which are "‘acquisition"’, "‘conversion"’, "‘readout"’ and "‘top manager"’. Actually, PARISROC is based on 2 memories. During acquisition, discriminated analog signals are stored into an analog memory (the SCA: switched capacitor array). The analog to digital conversion module converts analog charges and times from SCA into

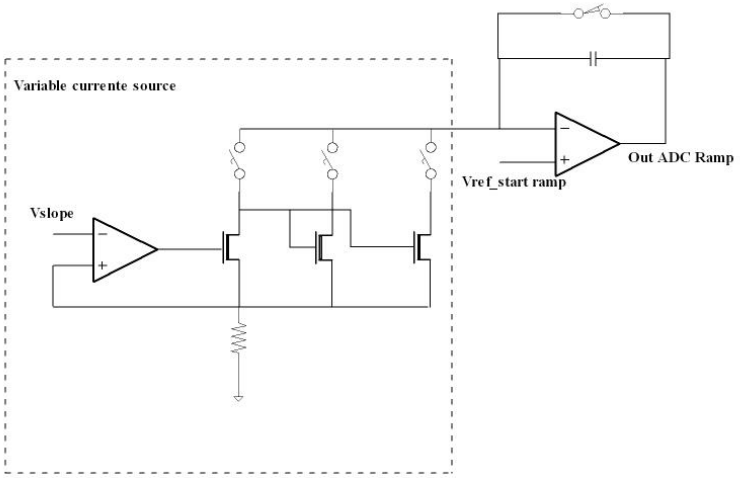

Figure 23. ADC ramp schematic.

12 bits digital values. These digital values are saved into registers (RAM). At the end of the cycle, the RAM is readout by an external system. The block diagram is given on Fig. 24.

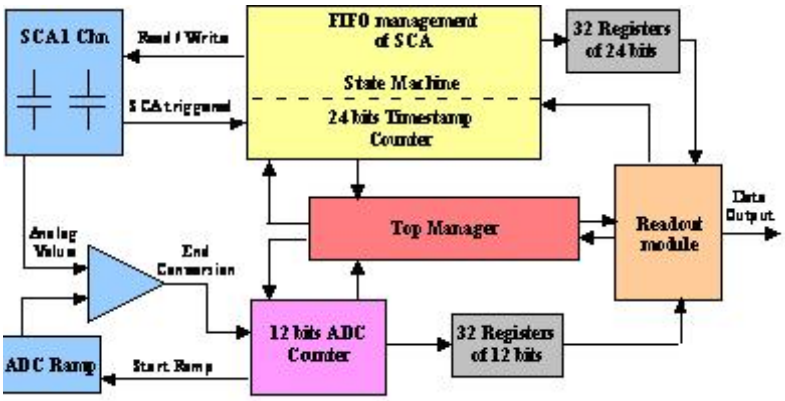

Figure 24. Block diagram of the digital part.

This sequence is made thanks to the top manager module which controls the 3 other ones. When 1 or more channels are hit, it starts ADC conversion and then the readout of digitized data. The maximum cycle length is about 200 μs. During conversion and readout, acquisition is never stopped. It means that discriminated analog signals can be stored in the SCA at any time of the sequence shown in on Fig. 25.

The first module in the sequence is the acquisition which is dedicated to charge and fine time measurements. It manages the SCA where charge and fine time are stored as a voltage like. It also integrates the coarse time measurement thanks to a 24-bit gray counter with a resolution of 100 ns. Each channel has a depth of 2 for the SCA and they are managed individually. Besides, SCA is treated like a FIFO memory: analog voltage can be written, read and erased from this memory.

Then, the conversion module converts analog values stored in the SCA (charge and fine time:

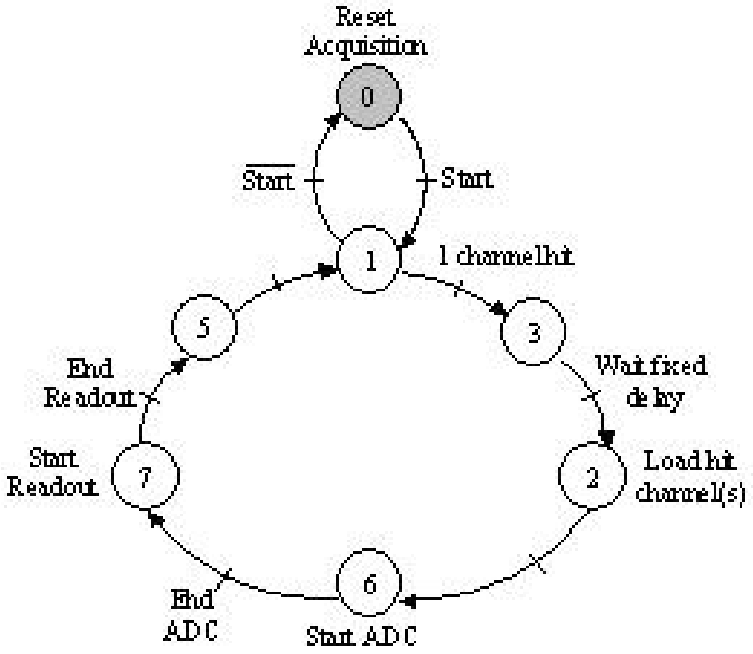

Figure 25. Top manager sequence.

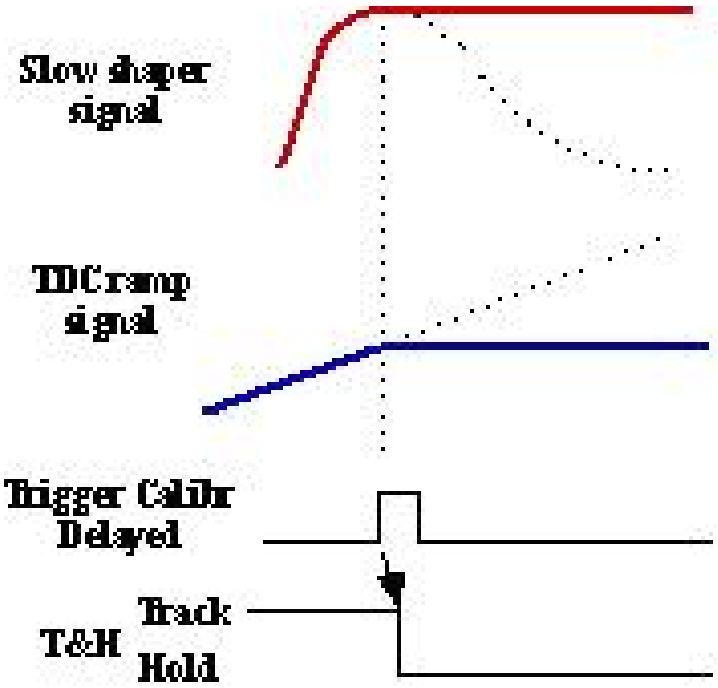

Figure 26. SCA analogue voltage

cf. ŕefFigfig:26) in digital ones thanks to a 12-bit Wilkinson ADC. The counter clock frequency is 40 MHz, it implies a maximum ADC conversion time of 103 μs when it overflows. This module

makes 32 conversions in 1 run (16 charges and 16 fine times).

Finally, the readout module permits to empty all the registers to an external system. As it will only transfer hit channels, this module will tag each frame with its channel number: it works as a selective readout. The pattern used is composed of 4 data: 4-bit channel number, 24-bit coarse time, 12-bit charge and 12-bit fine time. The total length of one frame is 52 bits. The maximum readout time appears when all channels are hit. About 832 bits of data are transferred to the concentrator with a 10 MHz clock: the readout takes about 100 μs with 1 μs between 2 frames.

3. ASIC Laboratory tests

The PARISROC has been submitted in June 2008; a first batch of 6 ASICs has been produced and received in January 2009 (a second batch of 14 ASICs in May 2009.

The ASIC test has been a critical step in the PARISROC planning due to the ASIC complexity.A dedicated test board has been designed and realized for this purpose (Fig. 27). Its role is to allow the characterization of the chip and the communication between photomultipliers and ASIC. This is possible thanks to a dedicated Labview program that allows sending the ASIC configuration (slow control parameters; ASIC parameters, etc) and receiving the output bits via a USB cable connected to the test board. The Labview is developed by LAL.

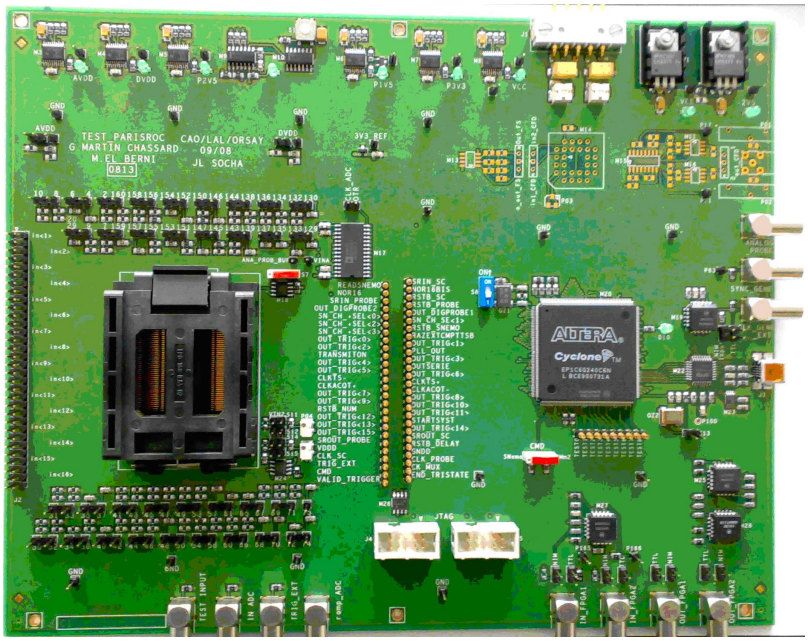

Figure 27. Test Board.

3.1 General tests

On Fig. 28 is shown the Test Bench used in laboratory. It is composed by a test board, a signal generator, an oscilloscope, multimeters and PC to run labview program.

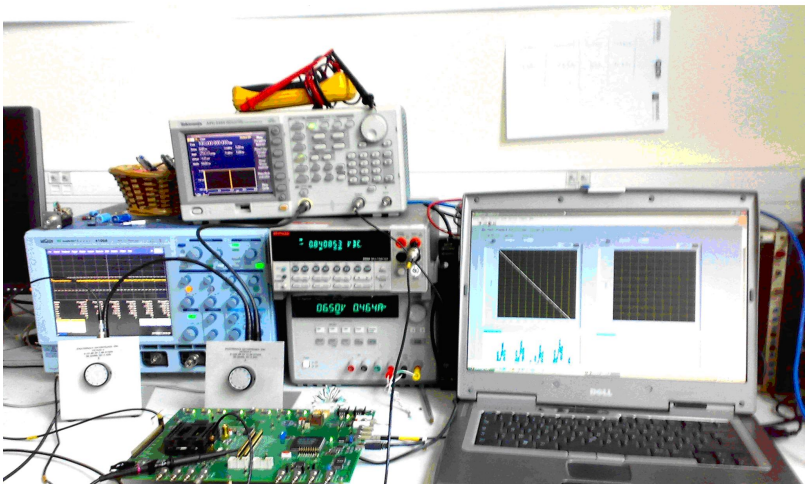

Figure 28. Test Bench.

The signal generator is a TEKTRONIX single channel function generator. It is used to create the input charge injected in the ASIC. The signal injected has the shaping as similar as possible to the PMT signal. On Fig. 28 is represented the generator input signal and its characteristics.

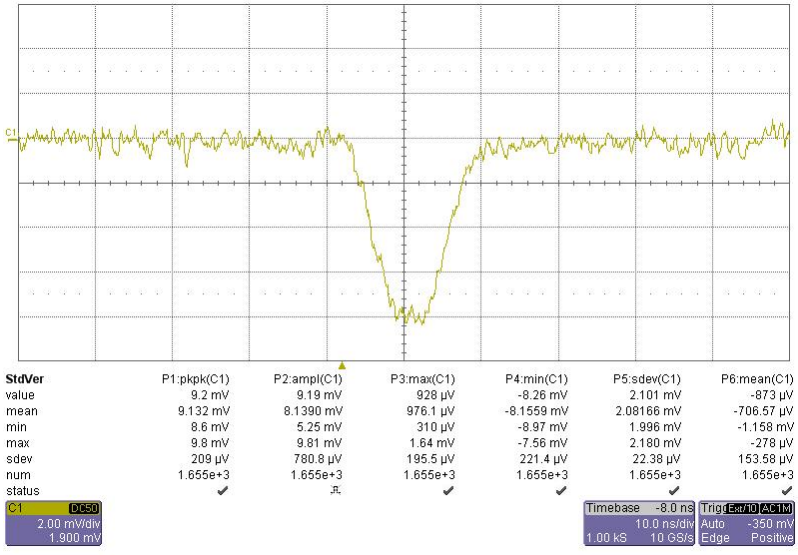

Figure 29. Input signals

At the beginning all the standard electrical characteristics have been tested: DC levels, analogue output signals, the analogue part characteristics and then the pedestals, the DAC linearity, Scurves (trigger efficiency as a function of the injected charge or the threshold), the ADC linearity. The first purpose is the comparison between simulation results and test measurements; most of

Table 7. TO BE COMPLETED

DC level	RMS
Preamplifier	3.8 mV (0.40 %)
Slow shaper	1.3 mV (0.10 %)
Fast shaper	1.0 mV (0.05%)

Table 8. TO BE COMPLETED. Preamplifier parameters.... $G_{pa} = 8$. WHY not same parameters 1 pe and 10 p.e

	Measurement	Simulation
Maximum voltage (10 pe)	50.00 mV	50.83 mV
Rise time (10 pe)	7.78 ns	4.79 ns
RMS noise	1 mV	0.47 mV
without USB cable	0.66 mV	
Noise in pe	0.2	0.086
without USB cable	0.132	
Maximum voltage (1 pe)	5.00 mV	5.43 mV
SNR (1 pe ????)	5	11.6
without USB cable	7.5	

them are in agreement with the ASIC characteristics, obtained in simulation.

3.2 Analogue tests

The DC level characterization is the first step in ASIC characterization; in particular the DC uniformity of the analogue part DC level for the different channels has to be measured.

In Fig. 30 are represented the preamplifier, slow shaper and fast shaper DC uniformity plots. The DC uniformity test has a small dispersion of 0.4%, 0.1% and 0.05% respectively for the preamplifier, the slow shaper and the fast shaper (Tab. 7).

The second step is the analogue part output signals: Injecting a charge equivalent to 10 pe, and setting a preamplifier gain at 8, are observed and compared with simulation results all the output waveforms.

There is a good agreement in preamplifier results (Fig. 31 and Tab. 8), the amplitude has the same value while time rise value has a difference of 3 ns. This difference is due to the output buffer placed in the test board.

The slow shaper waveforms are shown in Fig. 32 while Tab. 9 summarizes the results. The first differences appear: a different value in amplitude for slow shaper signal and fast shaper signal that is probably associate, also, to the Output Buffer. The second relevant difference is in noise value, in particular in slow shaper noise performance (Tab. 9).

The Fast shaper results are shown in Fig. 33 and Tab. 10.

Another important characteristic is the linearity. The output voltage in function of the input injected charge is plotted for the different analogue signals. Fig. 34 gives few examples for the preamplifier at different gains. Tab. 11 summarizes the fit results of these linearities. Good linearity

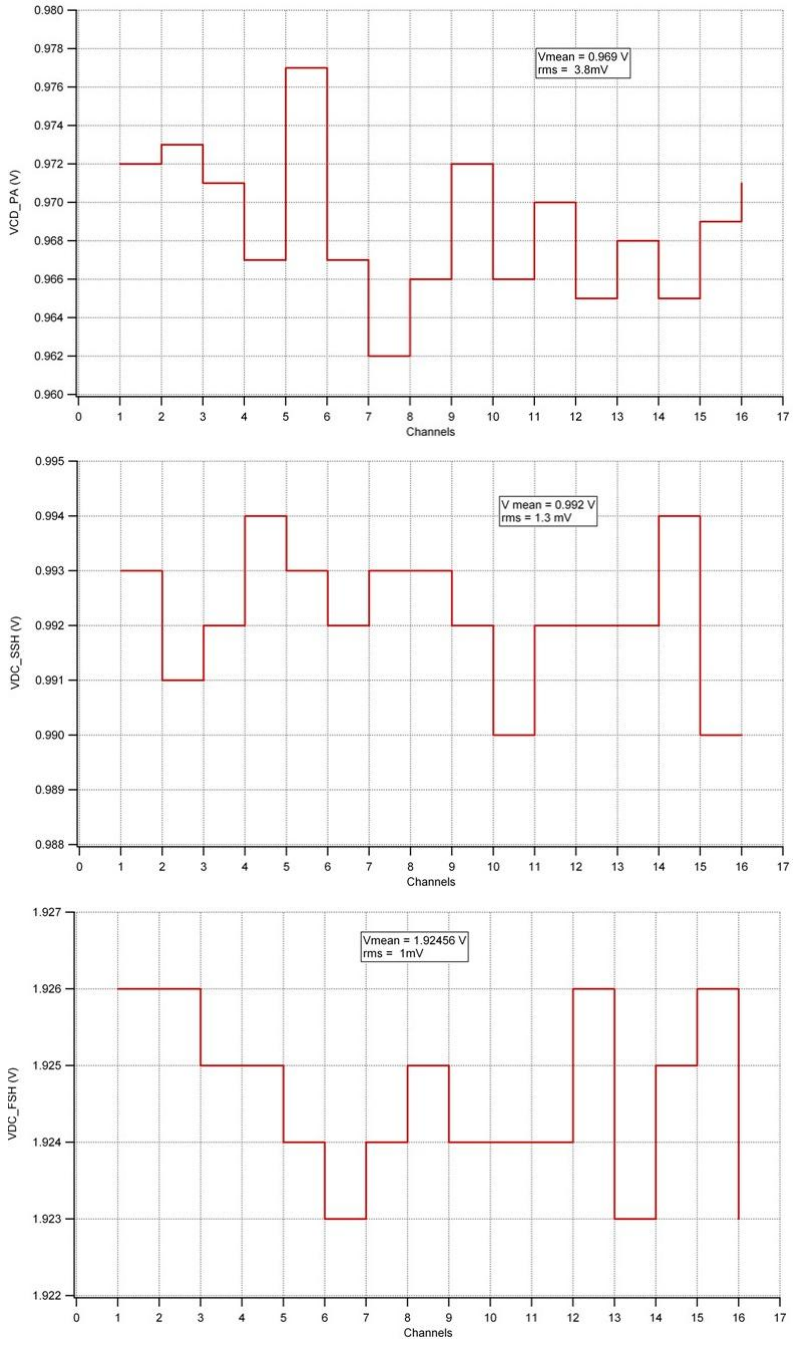

Figure 30. DC uniformity.

performances are shown by residuals (better than ± 2 %) value but for a smaller dynamic range than simulation.

Fig. 35 represents an example of slow shaper linearity for a time constant of 50 ns and a preamplifier gain of 8 with residuals better than $pm1$ %.

Fig. 36 gives an example of the fast shaper linearity until an injected charge of 10 pe. Residuals better than ± 2 % are obtained.

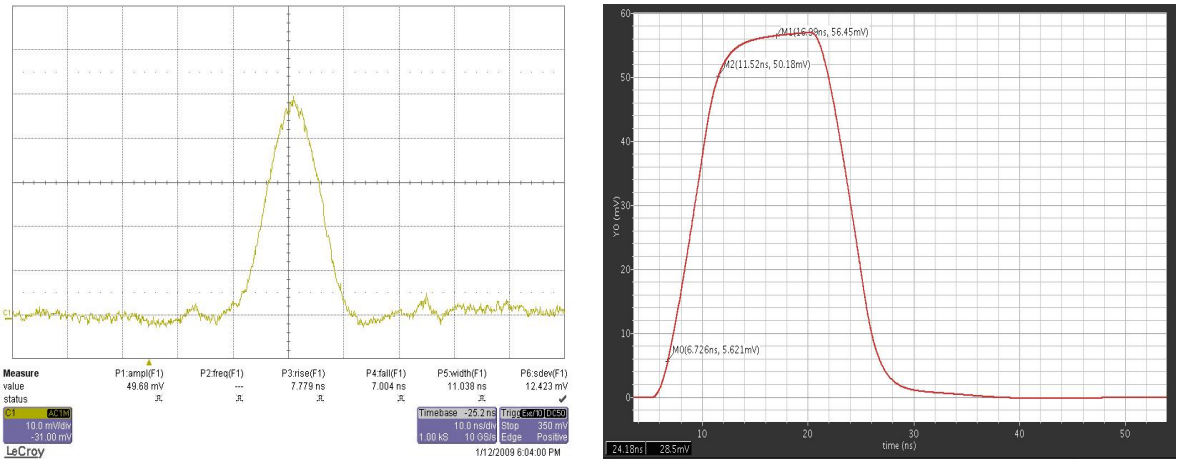

Figure 31. Measurement and simulation of the preamplifier output for an input charge of 10 pe.

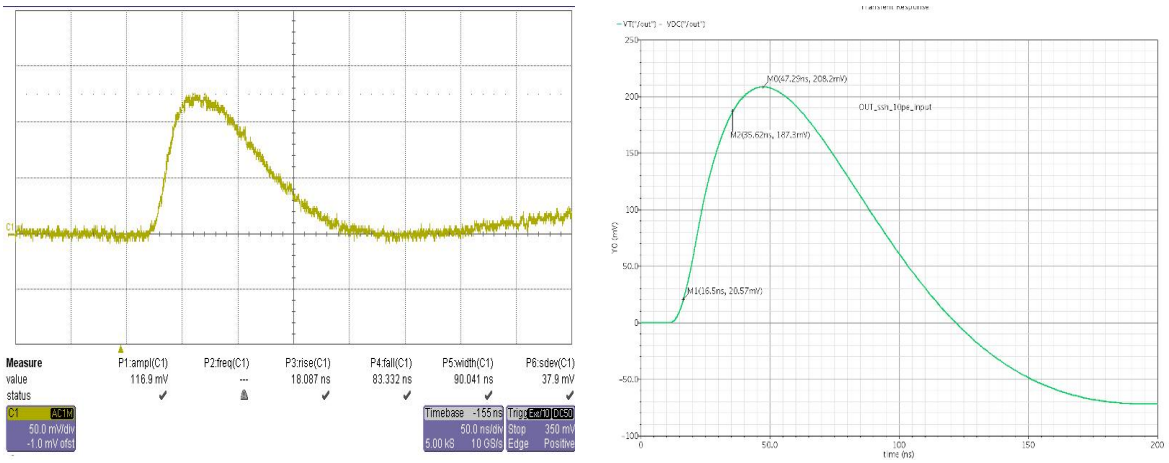

Figure 32. Measurement and simulation of the slow shaper output for an input charge of 10 pe.

Table 9. TO BE COMPLETED. $G_{pa} = 8$ and $RC = 50$ ns.

	Measurement	Simulation
Maximum Voltage (10 pe)	117 mV	290 mV
Rise time (10 pe)	18.0 ns	19.1 ns
RMS noise	4.0 mV	1.7 mV
Noise in pe	0.3	0.08
Maximum Voltage (1 pe)	12 mV	19 mV
SNR	3	11

The preamplifier linearity in function of variable feedback capacitor value with an input charge of 10 pe and with residuals from -2.5 % to 1.4 % is represented on Fig. 37 . The gain adjustment linearity is nice at 2 % on 8 bits.

On Fig. 38 is given the gain uniformity. For the different preamplifier gains is plotted the maximum voltage value for all channels in order to investigate the homogeneity among the whole

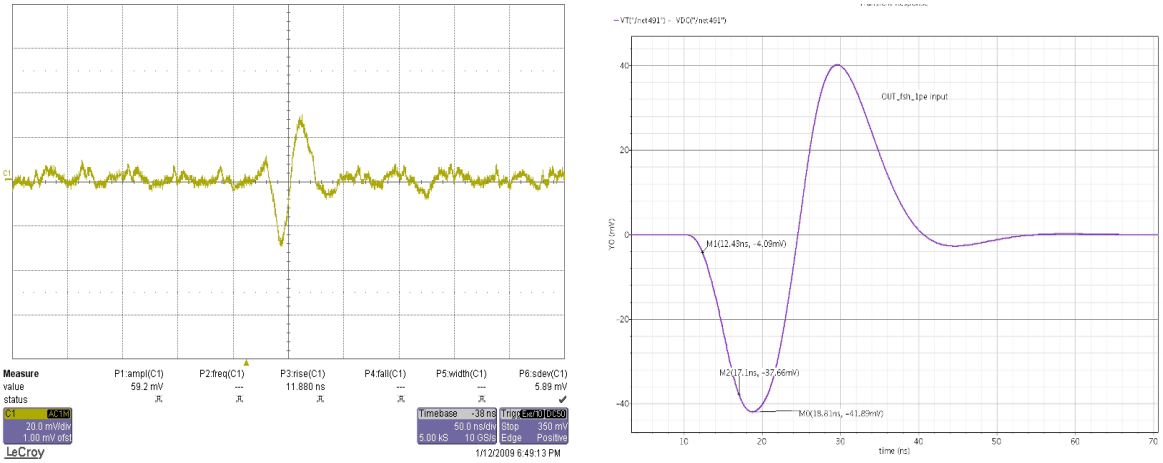

Figure 33. Measurement and simulation of the fast shaper output for an input charge of 1 pe.

Table 10. TO BE COMPLETED. $G_{pa} = 8$.

	Measurement	Simulation
RMS noise	2.5 mV	2.4 mV
Noise in pe	0.08	0.05
Maximum Voltage (1 pe)	30 mV	42 mV
SNR	12	18

Table 11. TO BE COMPLETED

Preamplifier Gains	Maximum voltage	Charge/Nb of pe	Residuals
8	0.52 V	12 pC / 78 pe	-1.0 % to 0.8 %
4	0.64 V	32 pC / 198 pe	-1.0 % to 1.0 %
2	0.51 V	50 pC / 312 pe	-2.0 % to 1.5 %

chip, essential for a multichannels ASIC. Residual dispersion of 0.05 %, 0.013 % and 0.012 % have respectively been obtained for gain 8, 4 and 2.

3.3 DAC linearity

The DAC linearity has been measured and it consists in measuring the voltage DAC (V_{dac}) amplitude obtained for different DAC register values. Fig. 39 gives the evolution of V_{dac} as a function of the register for the two DACs and residuals from -0.1 % to 0.1 %.

3.4 Trigger output

The trigger output behavior was studied scanning the threshold for different injected charges. At first no charge was injected which corresponds to measure the fast shaper pedestal. The result is represented on Fig. 40 for each channel. The S-curves are superimposed meaning good homogeneity. The spread is of one DAC count ($LSBDAC = 1.78$ mV) or 0.06 pe.

The trigger efficiency was then measured for a fixed injected charge of 10 pe. On Fig. 41 are represented the S-curves obtained with 200 measurements of the trigger for all channels varying

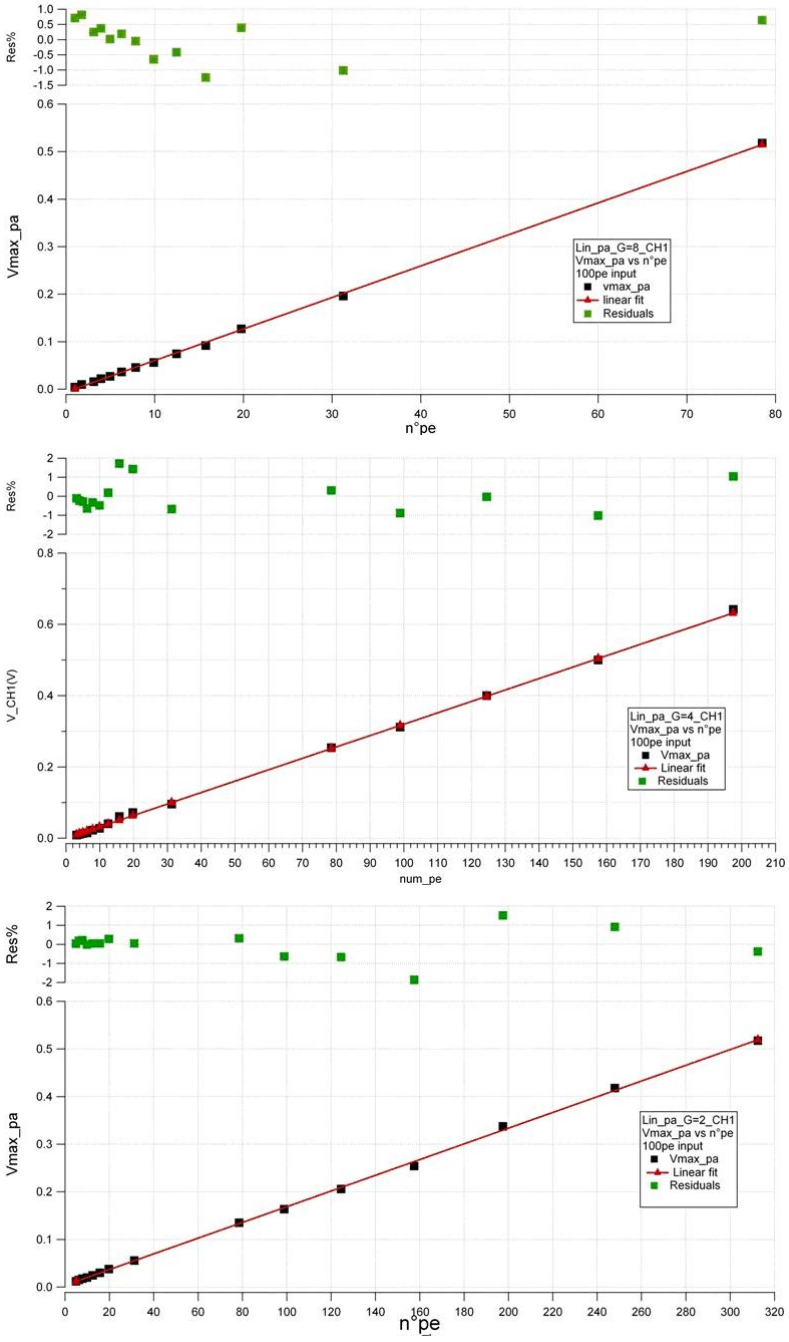

Figure 34. Preamplifier linearity for different gains.

the threshold. The homogeneity is proved by a spread of 7 DAC unit (0.4 pe) and a noise of 0.07 pe ($RMS = 2.19$).

The trigger output is studied also by scanning the threshold for a fixed channel and changing the injected charge. On Fig. 42 on the left panel is shown the trigger efficiency versus the DAC unit and on the right panel is plotted the threshold versus the injected charge but only until 0.5 pC. From these measurements a noise of 10 fC has been extrapolated. Therefore the threshold is only

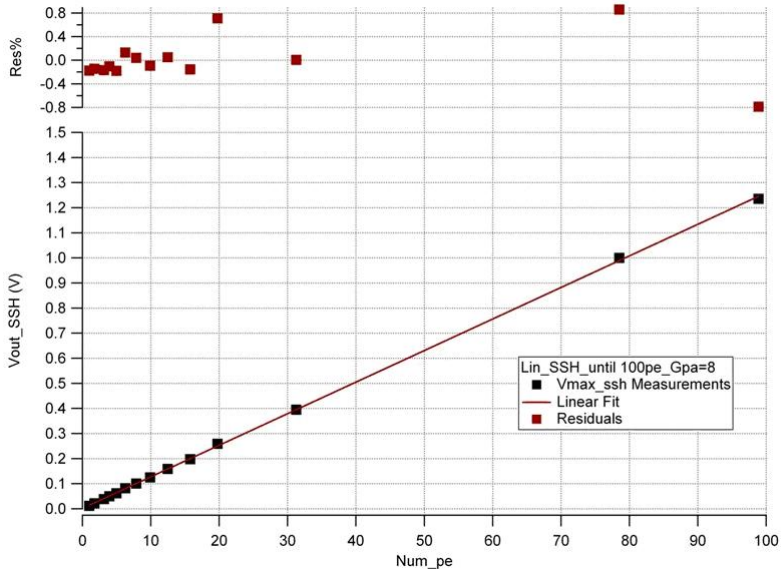

Figure 35. Slow shaper linearity; $RC = 50$ ns and $G_{pa} = 8$.

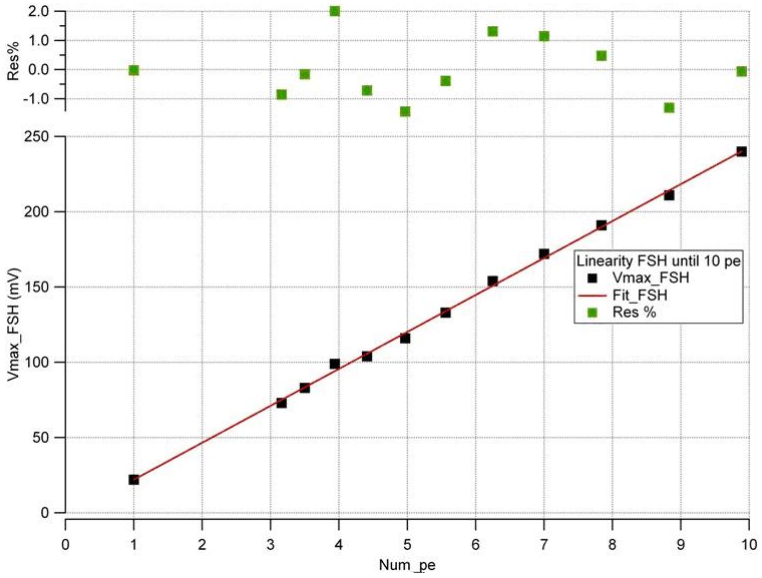

Figure 36. Fast shaper linearity up to 10 pe.

possible above 10 σ of the noise due to the discriminator coupling (Fig. 43).

The trigger coupling illustrated in Fig. 44 with the injected charge in channel 1 and output signal observed in channel 2, shows a coupling signal around 25 mV (10 fC). This coupling signal is due, probably, to the input power supply (V_{dd-pa} and V_{ss}).

3.5 ADC characterisation

The ADC performance has been studied alone and with the whole chain. Injecting to the ADC input directly a DC voltage by the internal DAC, in order to have a voltage level as stable as possible,

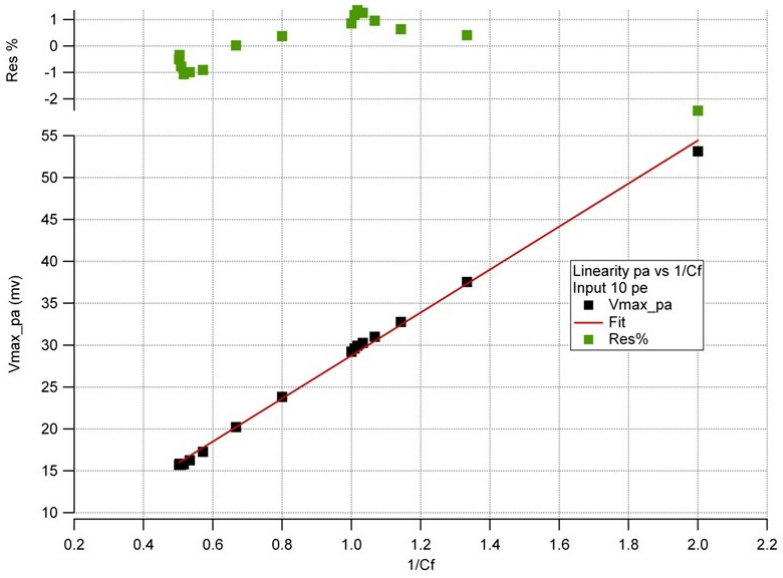

Figure 37. Preamplifier linearity vs feedback capacitor value.

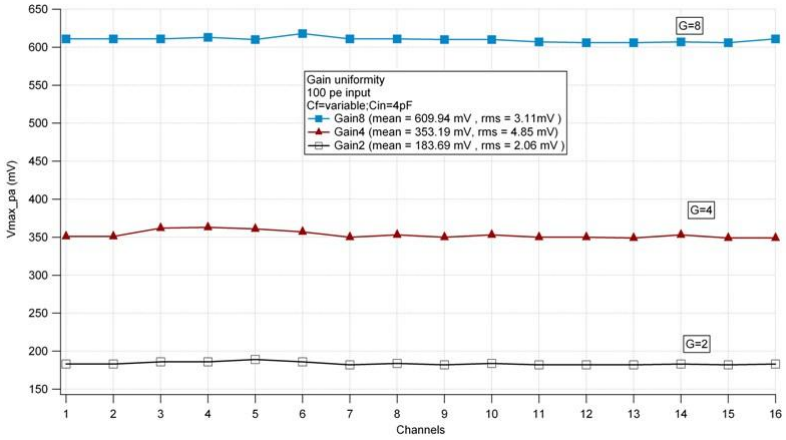

Figure 38. Gain uniformity for $G_{pa} = 8, 4, 2$.

were measured the ADC values for all channels (Fig. 45).

The measurement is repeated 10000 times for each channel and in the first plot of the LabView front panel window (Fig. 45). The minimal, maximal and mean values, over all acquisitions, for each channel are plotted. In the second plot there is the rms charge value versus channel number with a value in the range $[0.5, 1]$ ADC unit. Finally the third plot shows an example of charge amplitude distribution for a single channel: a spread of 5 ADC counts is obtained.

The ADC is suited to a multichannel conversion so the uniformity and linearity are studied in order to characterize the ADC behaviour. On Fig. 46 is represented the ADC transfer function for the 10-bit ADC versus the input voltage level. All channels are represented and have plots superimposed.

The good homogeneity observed is confirmed by the linear fit parameters comparison. In are

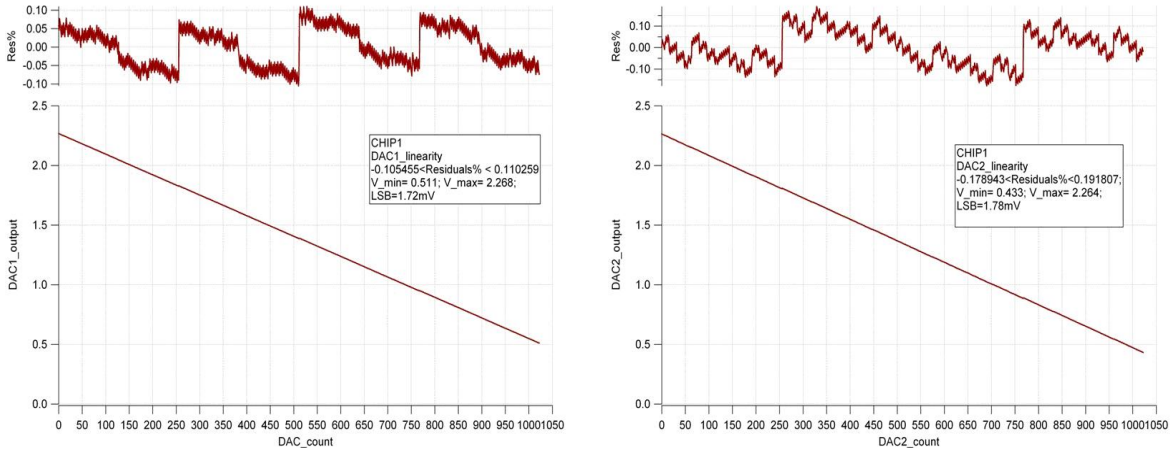

Figure 39. DAC linearity; DAC1 and DAC2 respectively.

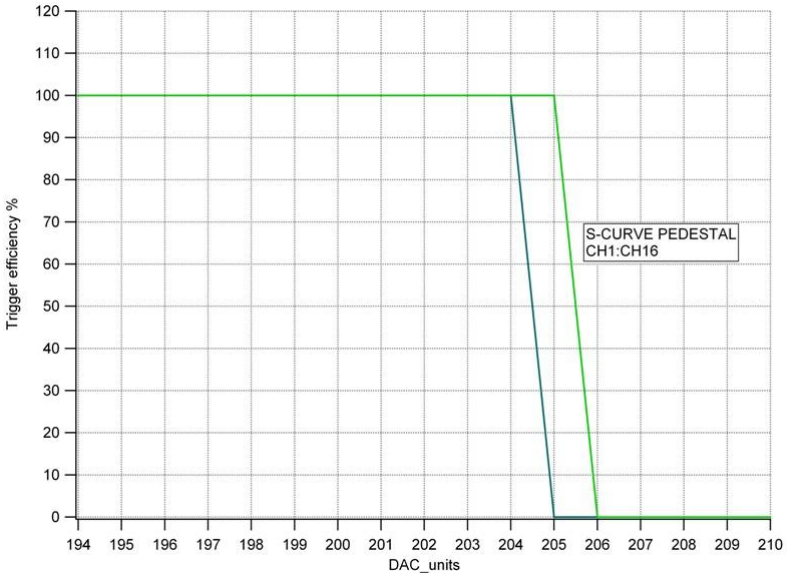

Figure 40. Pedestal S-curves for channel 1 to 16.

Table 12. TO BE COMPLETED. 10 bits ADC parameter fits.... 25 acquisitions per channel, $LSB = 1.06$ mV...

	Slope	Intercept
Mean	936.17	859.8
RMS	0.14	0.3

plotted the slope and the intercept distributions for all channels. The RMS slope value of 0.143 and the RMS intercept value of 0.3 confirm the 10-bits ADC uniformity (Tab. 12).

In Fig. 48 are shown respectively the 12, 10 and 8 bits ADC linearity plots with the 25 measurements made for each input voltage level. The average ADC count value is plotted versus the input signal. The residuals from -1.5 to 0.9 ADC units for the 12-bits ADC; from -0.5 to 0.4 for

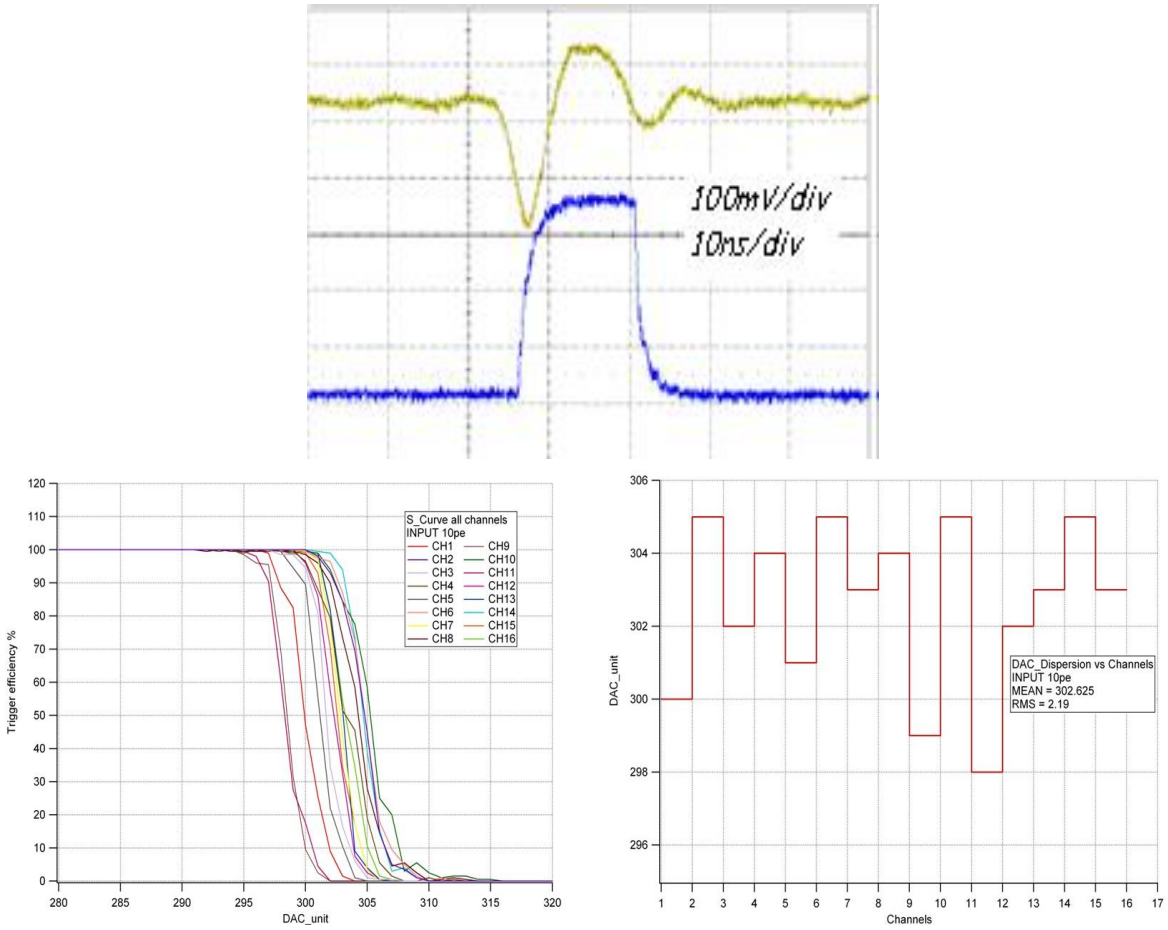

Figure 41. Fast shaper and trigger (top panel); S-curves for input of 10 pe (left panel); uniformity plot for channel 1 to 16 (right panel).

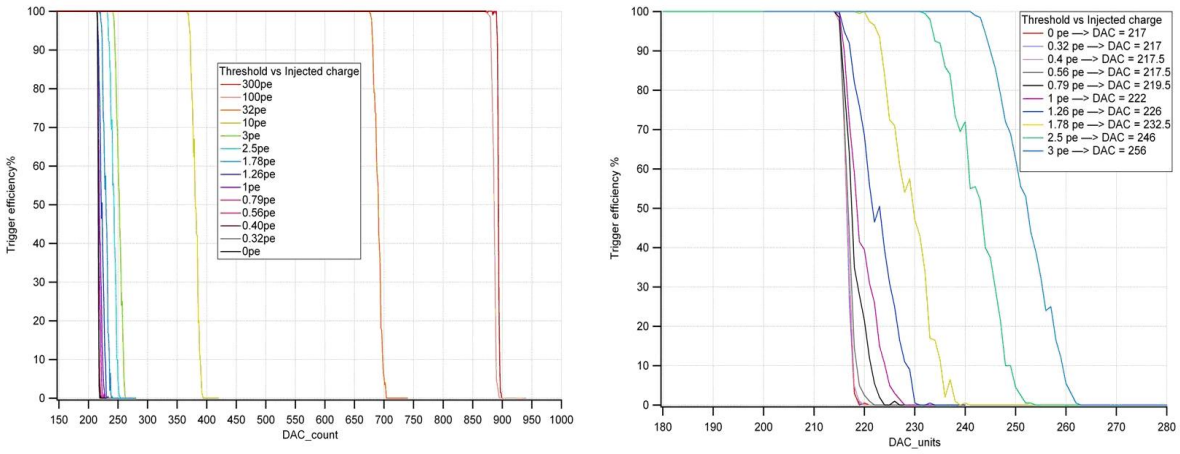

Figure 42. Trigger efficiency vs DAC count up to 300 pe (left panel) and until 3 pe (right panel).

the 10-bit ADC and from -0.5 to 0.5 for the 8-bit ADC. This prove the good ADC behaviour in terms of Integral non linearity.

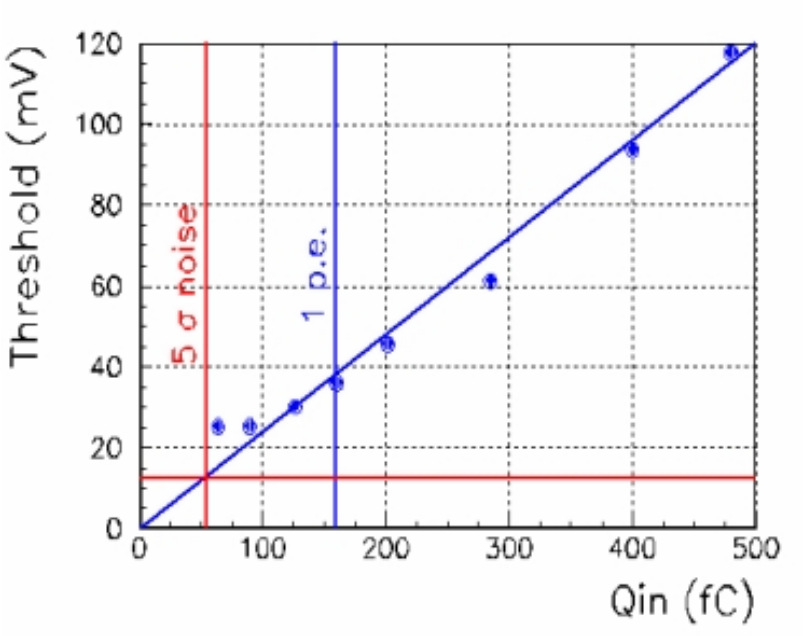

Figure 43. Threshold vs injected charge up to 500 fC. It is shown the 1 p.e threshold for a PMT gain of 10^6.

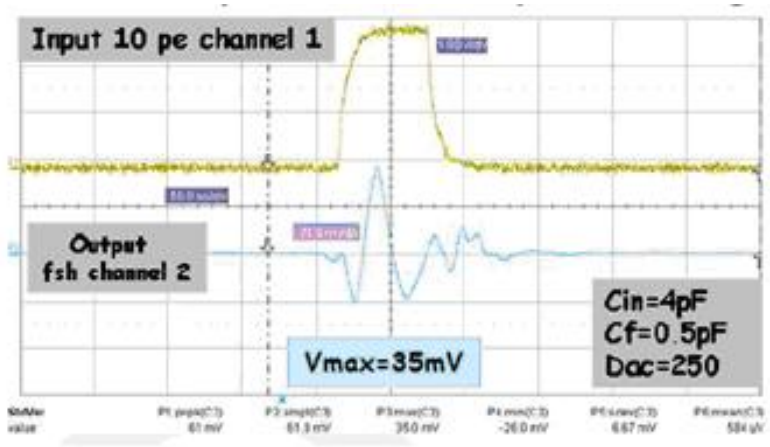

Figure 44. Trigger coupling signal.

In terms of Differential non linearity, the value from -1.0 to 0.65 for the 10 bit ADC and from -0.3 to 0.2 for the 8 bit ADC, show us a good behaviour even if the plots are the results of preliminary measurements.

Once the ADC performances have been tested separately, the measurements are performed on the complete chain. The results of the input signal autotriggered, held in the T&H and converted in the ADC are illustrated in where are plotted the 10-bit ADC counts in function of the variable input charge (up to 50 pe). A good linearity of 1.4 % and a noise of 6 ADC units are obtained. In Tab. 13 are listed the setting value for measurements.

On Fig. 51 is plotted the 8-bit linearity at 1.4 % and a noise of 1.53 ADC unit. In Tab. 13 are listed the setting value for measurements.

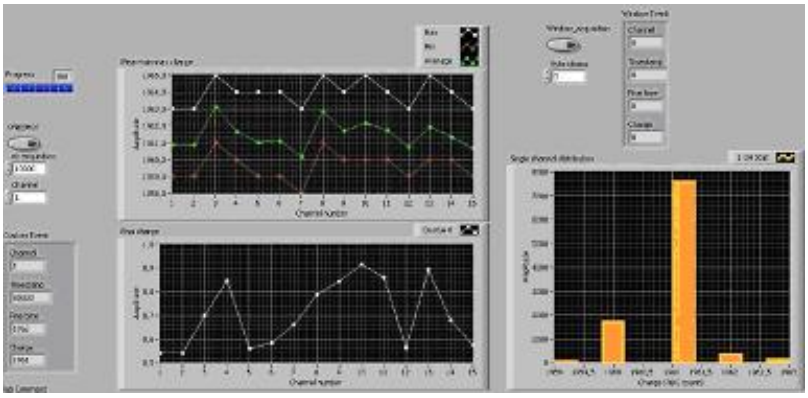

Figure 45. ADC measurements with DC input 1.45 V (middle scale).

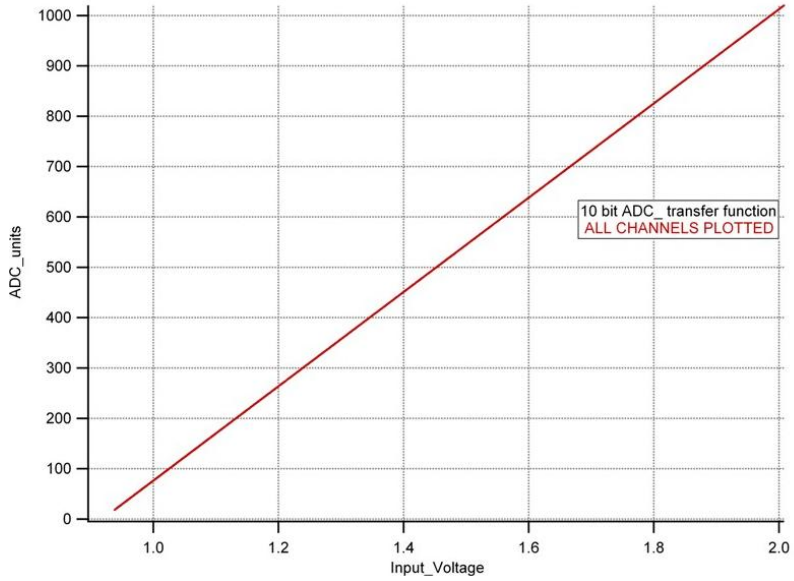

Figure 46. 10 bits ADC transfer function vs input charge.

Table 13. TO BE COMPELTED. $G_{pa} = 14$ ($C_{in} = 7$ pF , $C_f = 0.5$ pF), Slow shaper $RC = 50$ ns, DAC delay: $bit < 0 >= 1$ & $bit < 2 >= 1$.

Parameters	12 bits ADC	10 bits ADC	8 bits ADC
LSB	0.27	1.06 mV	4.26 mV
Min ADC count at 3 pe	509	132	33
Max ADC count at 50 pe	3873	989	241
Residuals in ADC units	$[21,54]$	$[6,14]$	$[2,3]$

On Fig. 53 is plotted the 12-bit linearity at 1.4 % and a noise of 23.69 ADC unit. In Tab. 13 are listed the setting value for measurements.

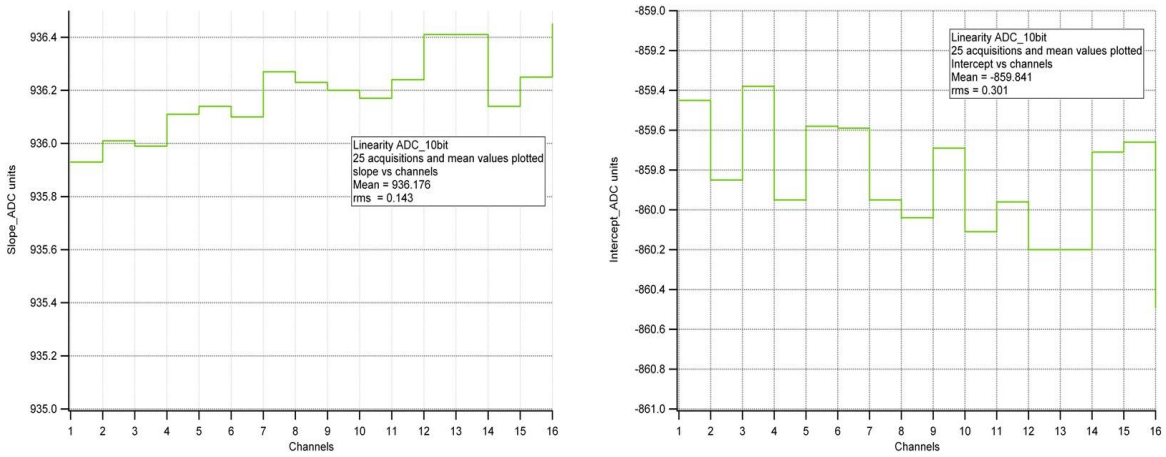

Figure 47. Evolution of the fit parameters (slope on the left panel and intercept on the right panel) as a function of the channel number.

4. Measurements with PMTs

The first measurements with a photomultiplier at input are started in IPNO at Orsay.

Acknowledgments

This work, especially one of the author, is supported by the National Reasaerch Agency under contract ANR-06-BLAN-0186.

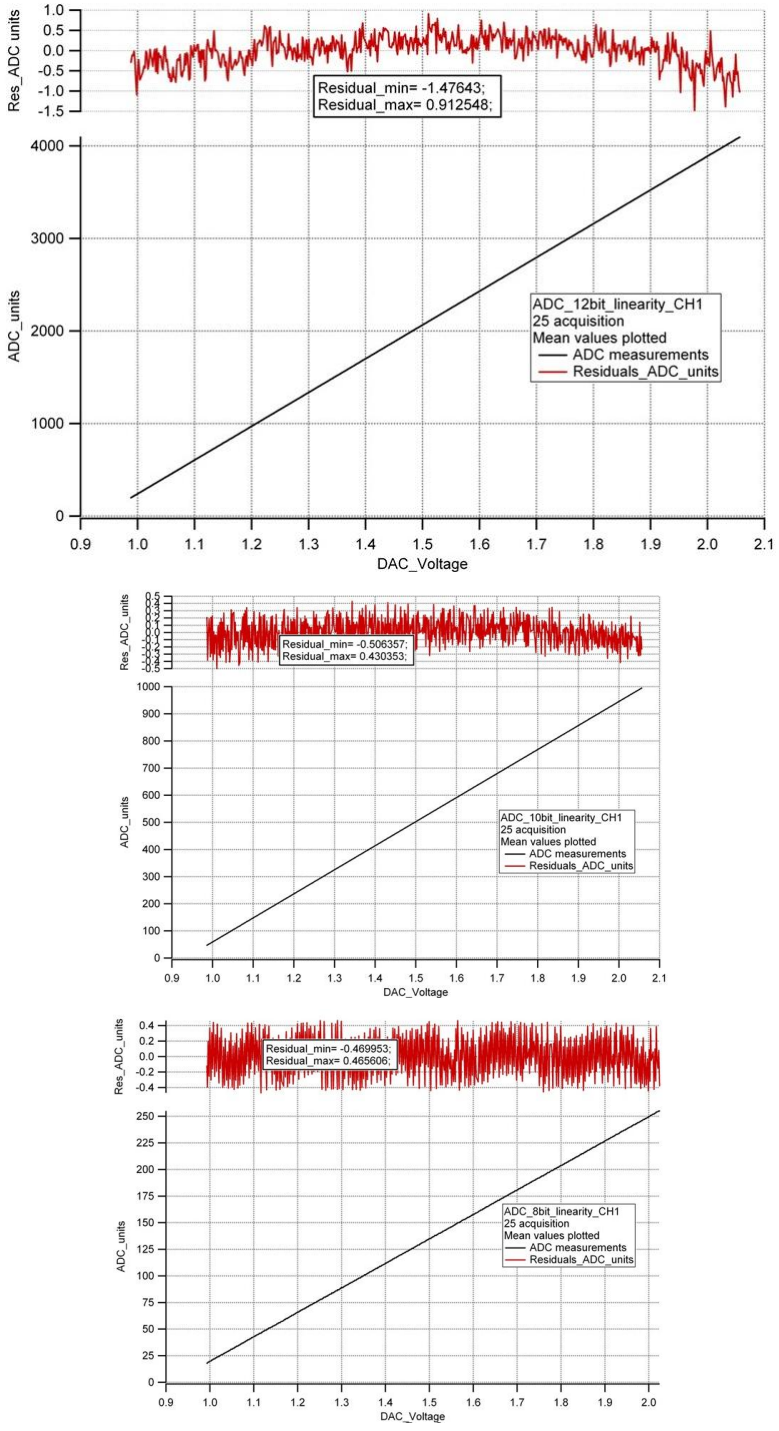

Figure 48. 12, 10, 8 bit ADC linearity.

References

[1] B. Genolini *et. al.*, "PMm2: large photomultipliers and innovative electronics for the next-generation neutrino experiments" 0811.2681.

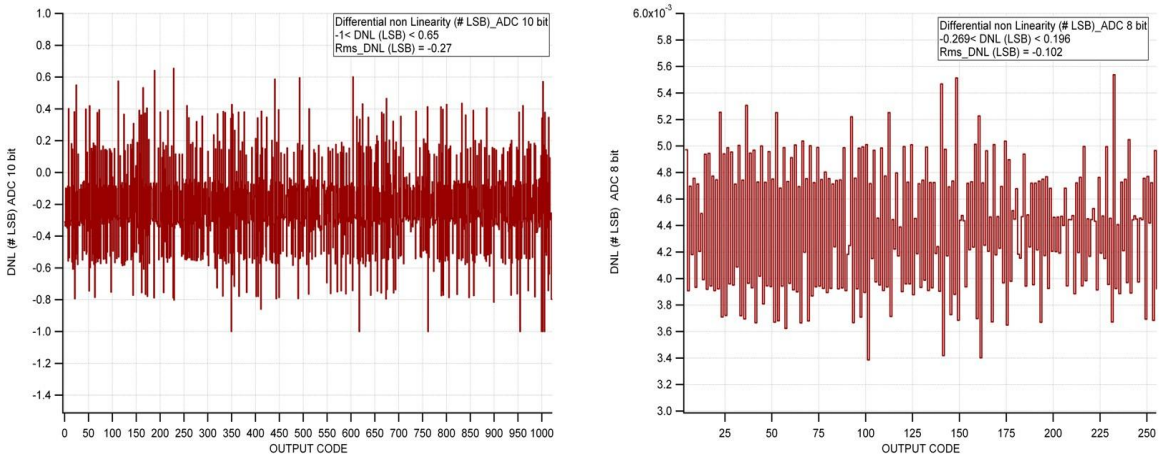

Figure 49. Differential non linearity.

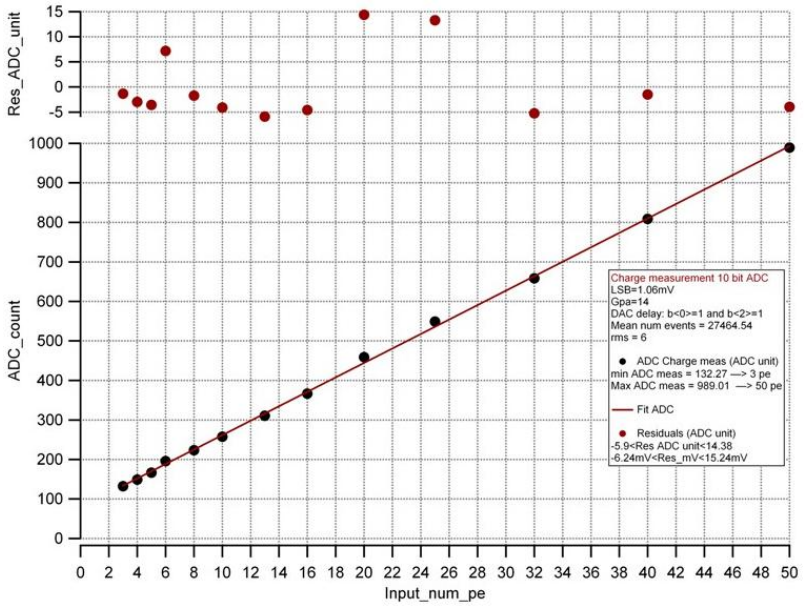

Figure 50. 10 bit ADC linearity.

[2] http://pmm2.in2p3.fr/.

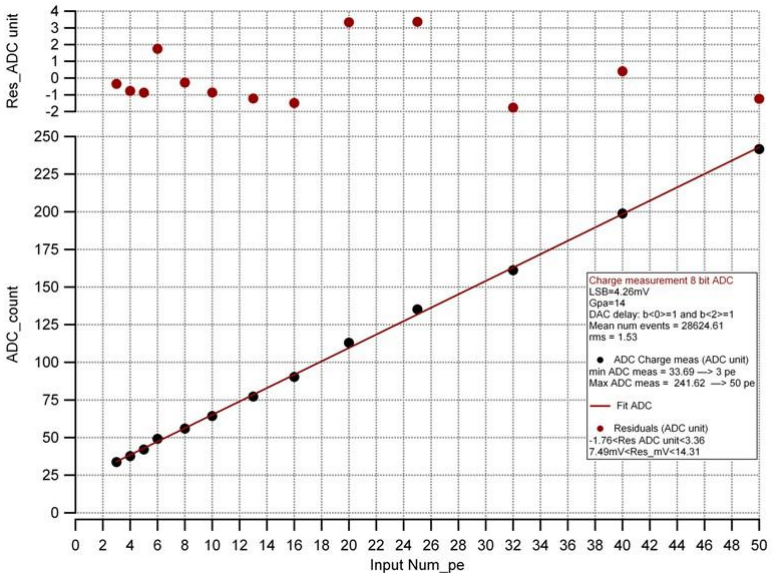

Figure 51. 8 bit ADC linearity.

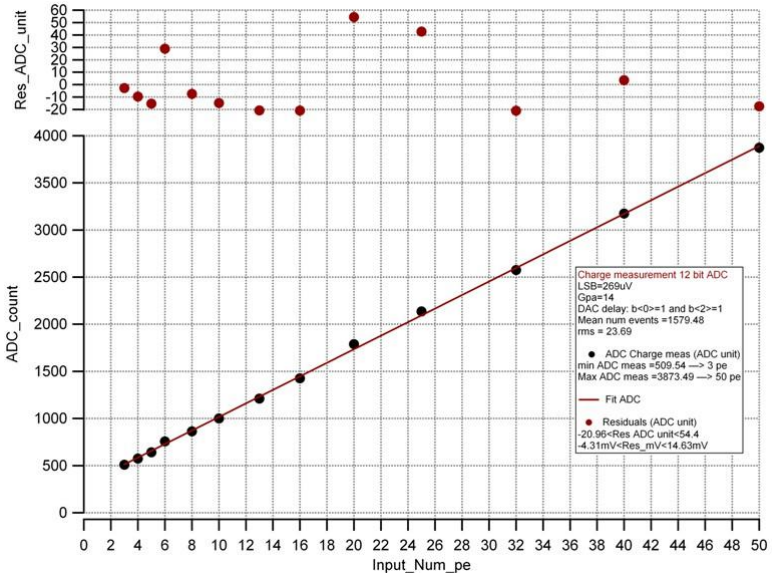

Figure 52. 12 bit ADC linearity.

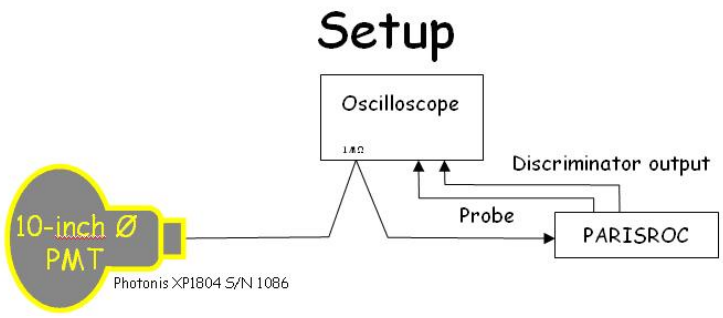

Figure 53. TO BE COMPLETED