

Status of FE Electronics

Arnaud Lucotte

for the experts:

C. de laTaille, G. Martin-Chassard

L. Raux, F. Mallet

Thanks to:

K. Borer and M. Hess

Content

- 1) FE chip design
 - a) Characteristics (reminder)

- 2) 32-channel Chip
 - a) Preamplifier
 - b) Auto-triggering
 - c) Charge measurement

- 3) Chip with improved features
 - a) Auto-triggering
 - b) Charge measurement

- 4) Next chip iteration
 - a) Version 1a and Version 2
 - b) Plans & Schedule

32-channel chip (Reminder)

Chip Design

- Complete chip with 32 channels + 2 test channels
 - Technology: AMS 0.8 μm BiCMOS
 - Ch01-32: 32 inputs / 1 trigger + 1 multiplexed output
 - Ch33 : powered separately / intermediate outputs
- Chip area :
 - $S=10 \text{ mm}^2$
- Package : QFP100

Preamplifier

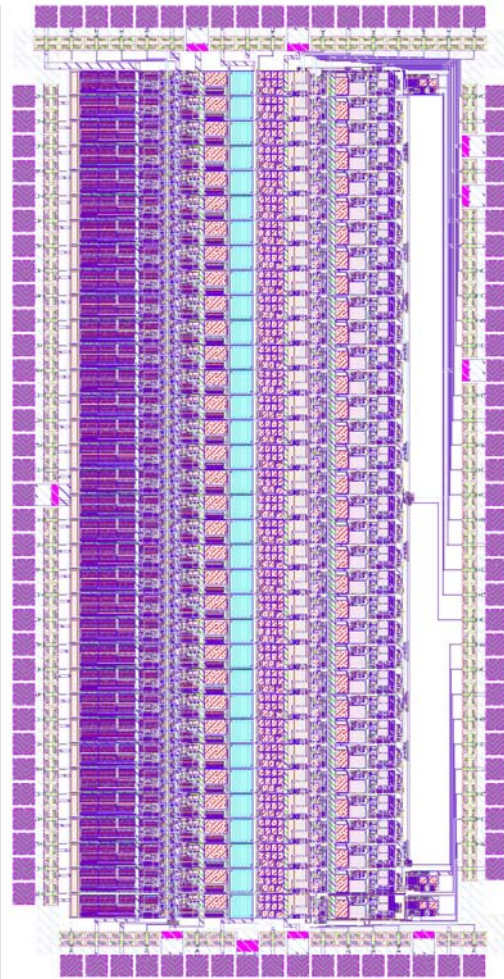
- Variable Gain preamp.
 - Current mirror architecture
 - Gain Range:[1, 1/2, 1/4, 1/8](4bits)

Auto-trigger

- Fast Shaper
 - Peak time $t_p = 10 \text{ ns}$
 - Gain $G \sim 20$
- Comparator

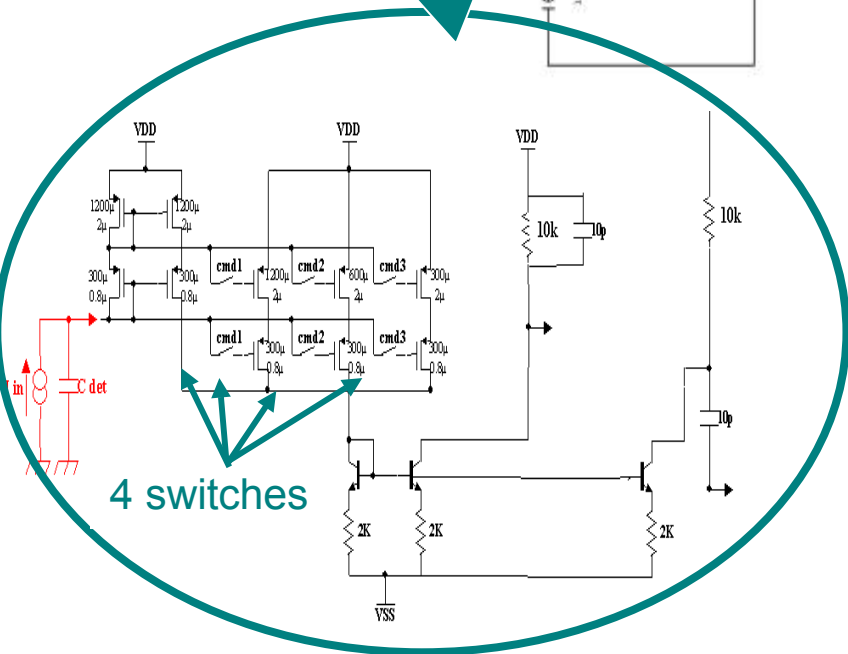
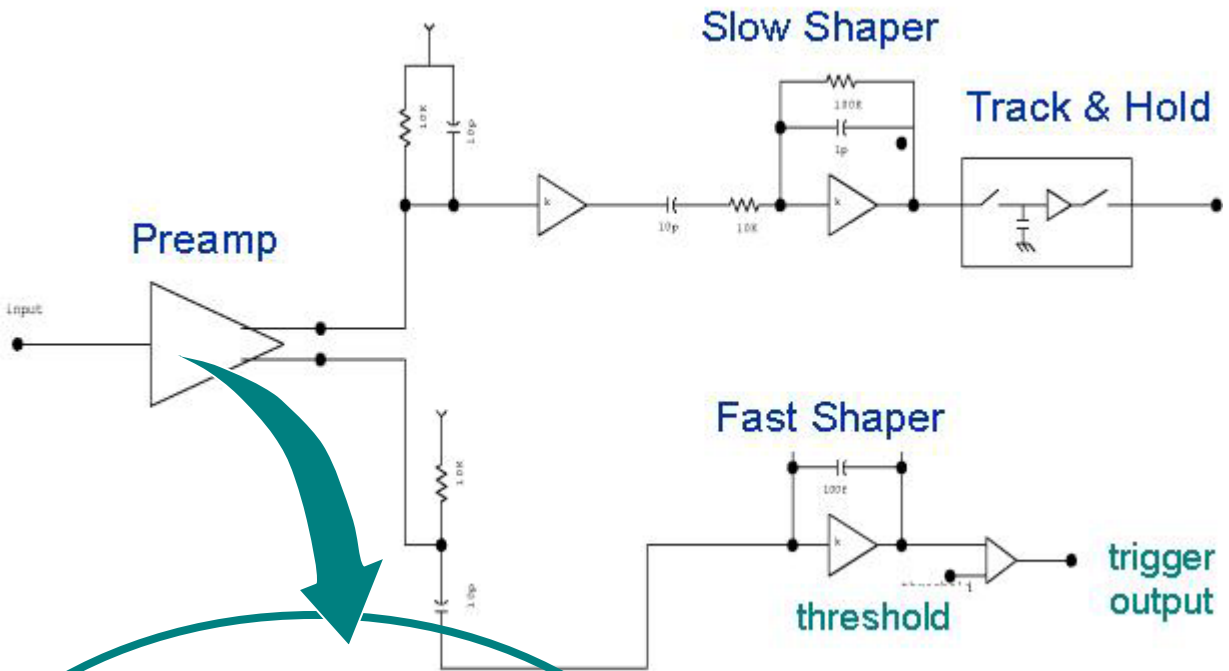
Charge Measurement

- Slow Shaper:
 - Peak time $t_p = 120 \text{ ns}$
 - Gain $G \sim 1$
- Track & Hold:
 - On chip track and hold
 - Output multiplexer
- Readout Frequency : 5MHz



Submitted FEB-02 / Received JUN-02
Tested JUN to SEP-02 at LAL and at Bern

One channel schematics (Reminder)



Tests performed on:

Preamplifier

Auto-Trigger:

- Fast Shaper
- Comparator

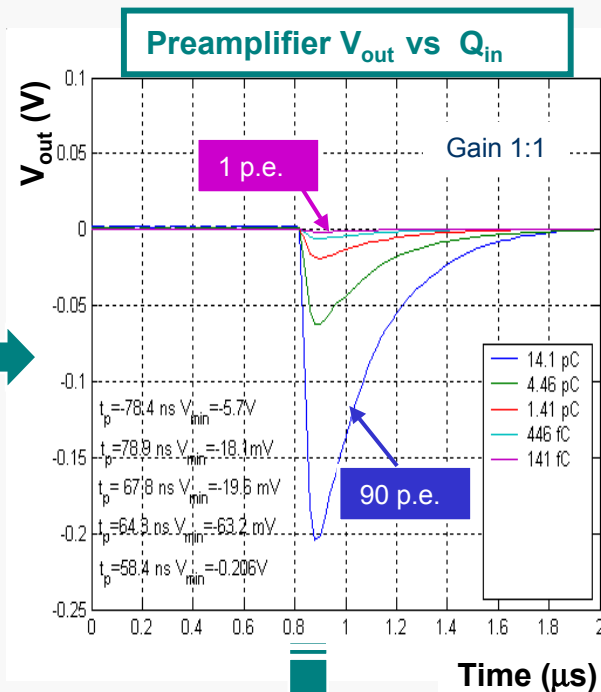
Charge Measurement:

- Slow Shaper
- Track & Hold

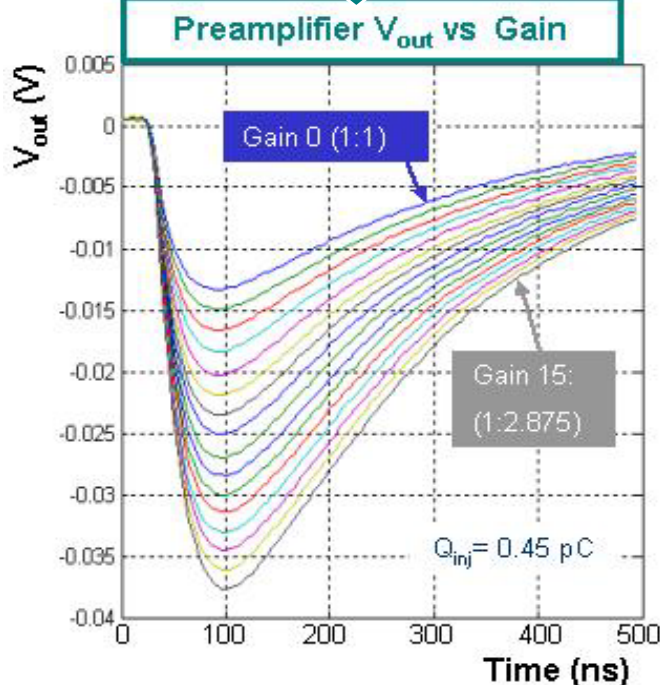
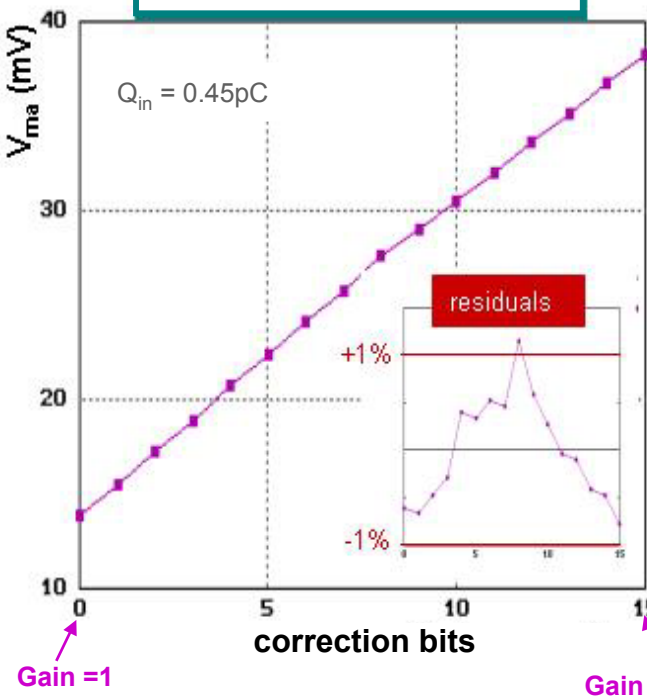
32-channel Chip Tests: Preamplifier

Preamplifier performance

- Preamp. Gain:
 - $G \sim 60 \text{ mV} / \text{pC}$ (#01-32)
 - $G = 25 \text{ mV} / \text{pC}$ (#33)
- Gain Correction:
 - Fully operational over the 1 to 2,875 range
- Gain Correction Linearity:
 - Better than $\sim 1\%$ over the whole range of correction



Gain Correction Linearity



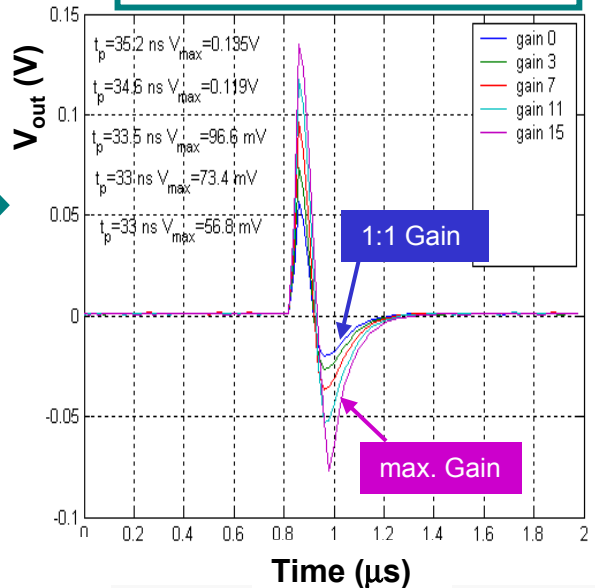
32-channel Chip Tests: Auto-trigger

Fast Shaper & Comparator

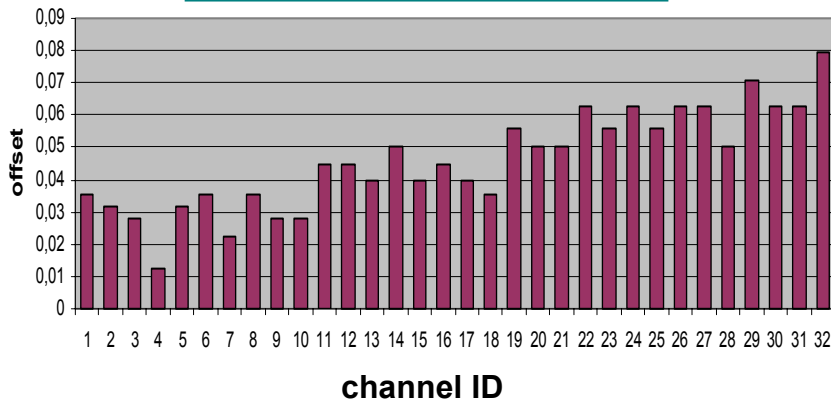
- Trigger capabilities:
 - $\epsilon \sim 100\%$ down to $1/2$ p.e.
- Fast Shaper Gain:
 - $G \sim 130$ mV / p.e.
- Fast Shaper Peaking time:
 - $t_p \sim 30$ ns (all)



Fast Shaper V_{out} vs Gain



Relative offset vs channel #



- Pedestal spread:
 - ~ 70 mV
 - 2 main sources:
 - Fast shaper (major)
 - Comparator (\sim negl.)
- Noise RMS :
 - ~ 1 mV

Remark

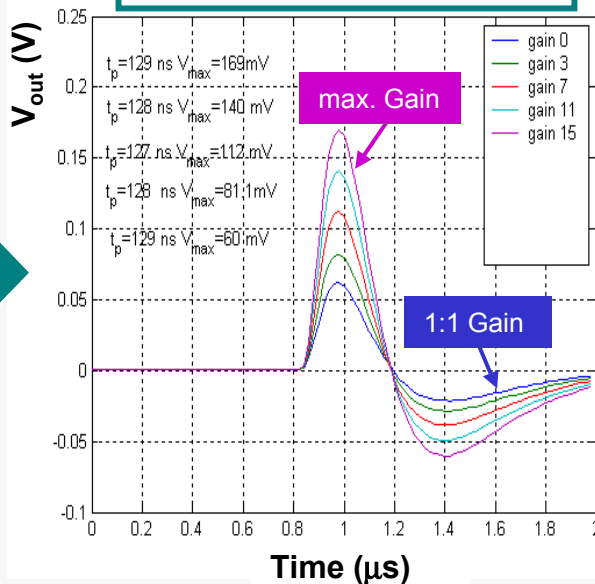
- Comparator issue:
 - Some design problem leads to the use of “ad hoc” fixes
 - This problem is now well identified & understood and will be fully solved with the next iteration (see Vers. 1a)

32-channel Chip Tests: Charge measurement

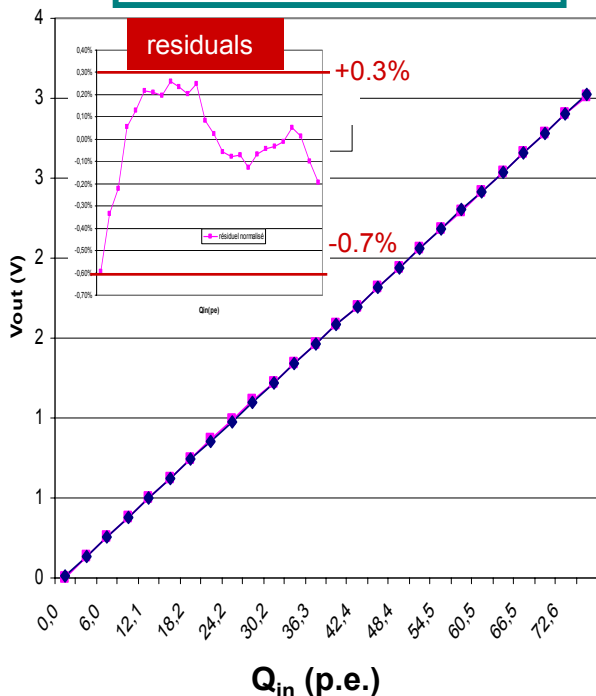
Measured Performance

- Dynamic Range :
 - [0-80]p.e.
- Slow shaper Gain
 - ~15-16 mV / pe (Gain 1)
- Slow Shaper peaking time:
 - $t_p \sim 100$ ns (#01-32)
 - $t_p \sim 130$ ns (#33)
- Track & Hold:
 - Fully operational
- Linearity:
 - < 1% over [1-80]p.e.

Slow Shaper V_{out} vs Gain

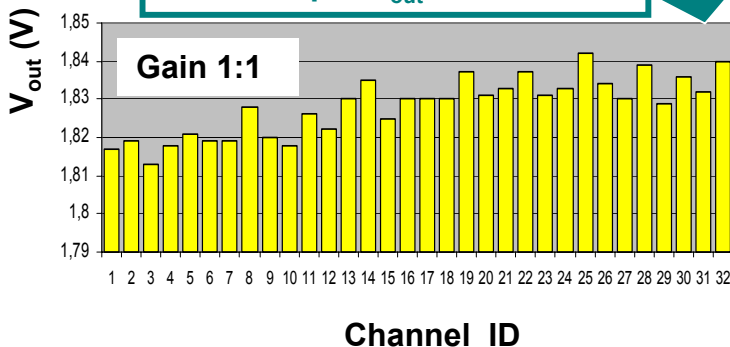


Slow Shaper Linearity



- Noise RMS :
 - RMS ~ 0.5 mV (0.02 pe)
 - Pedestal spread :
 - ~ 40 mV (~1 pe)
- Understood:
~50% from Shaper ,
~50% from Track and Hold

Slow Shaper V_{out} vs channel



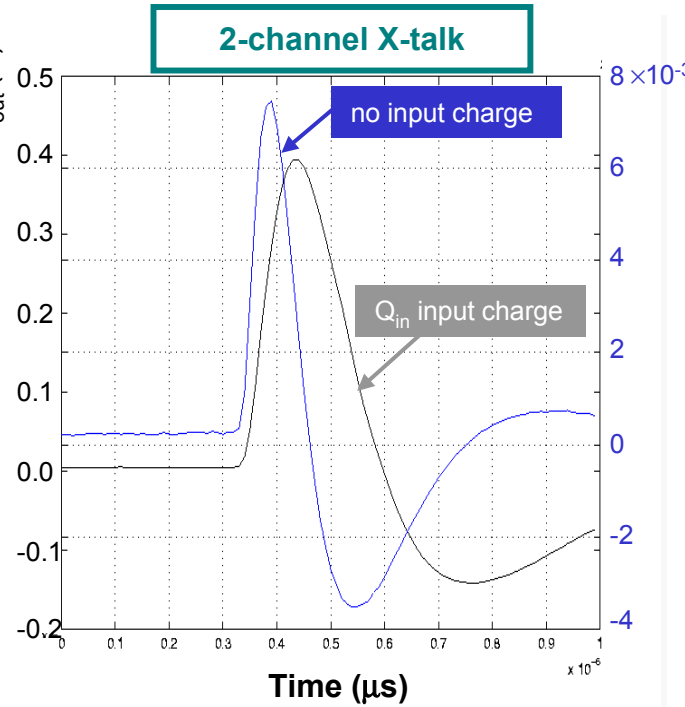
32-channel Chip Tests: Cross-Talk issue

Channel-to-Channel X-talk

- Measurements:
 - ~2%
- Main source:
 - Preamp “large” input $Z_{in} \sim 1.5 - 2.0 \text{ k}\Omega$

will be improved with reduced Impedance preamp. (see “Mecano” chip)

$V_{out} (V)$

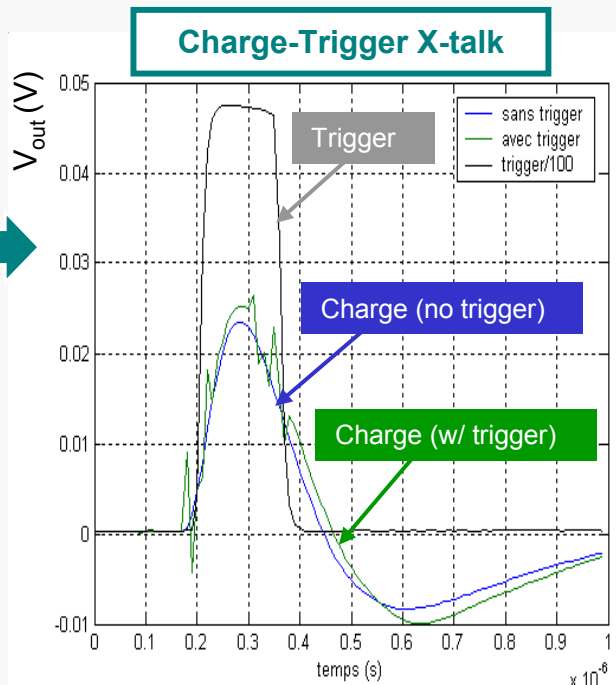


Trigger-Charge X-talk

- Cross talk Trigger and Charge Channel :
 - Capacitive coupling Injection charge in all channels

X-talk expected to be well reduced with new chip

$V_{out} (V)$



32-channel Chip Tests: summary

Internal note in preparation

	32-channels chip	mecano chip
Auto Trigger:		
Pedestal spread	80 mV	
Noise RMS	1 mV (<< 1.p.e.)	
Comparator	fixed	
Fast Shaper t_p	$t_p=35$ ns	
Fast Shaper Gain	130 mV / p.e	
Charge meas:		
Dynamic range	[0-80] p.e.	
Gain Correction	Operational (4 bits)	
Pedestal spread	40 mV	
Noise RMS	0.5 mV (<<1.pe.)	
Slow Shaper t_p	$t_p=100$ ns	
Slow Shaper Gain	16 mV / p.e.	
Cross-talk	O(2%)	

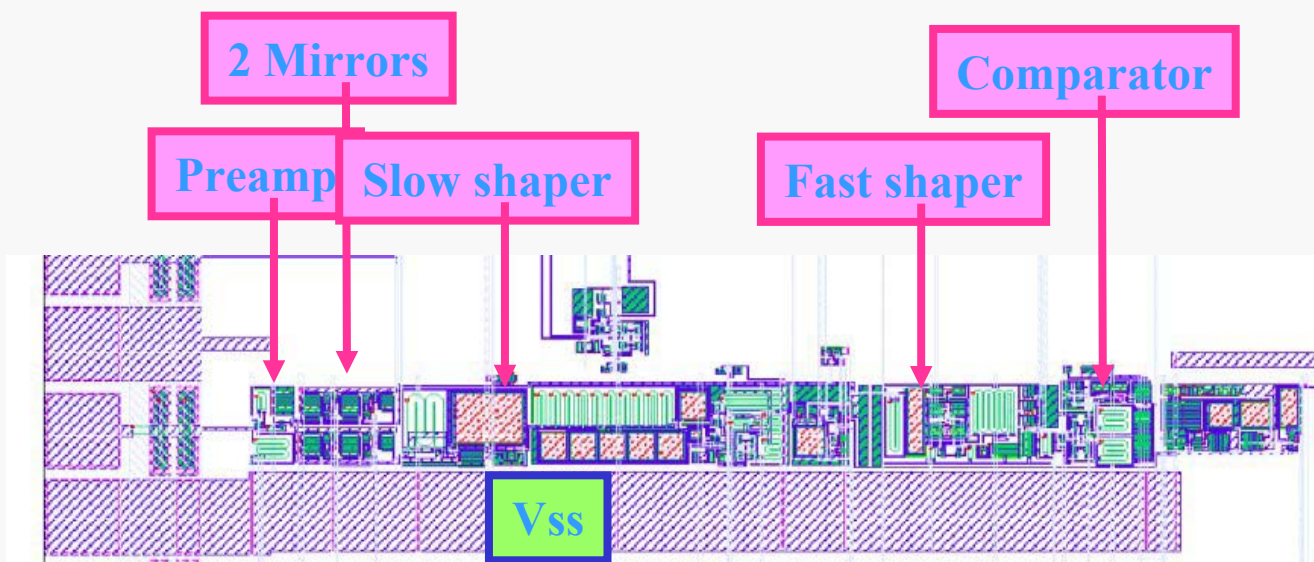
Chip with extra feature: Mecano Chip

Main new features:

- New variable gain preamplifier :
 - Low Impedance $Z_{in} \sim 70 \Omega$
 - Range 1-3 , 2 bits resolution (1,1/2)
- New Differential PMOS Fast shaper
 - $t_p = 10 \text{ ns}$
 - $G \sim 20$
- New Differential Slow shaper
 - $t_p = 120 \text{ ns}$
 - $G \sim 1$
- On chip Track & Hold and output multiplexer
 - Power consumption : 1.6 mW

reduce current,
X-talk

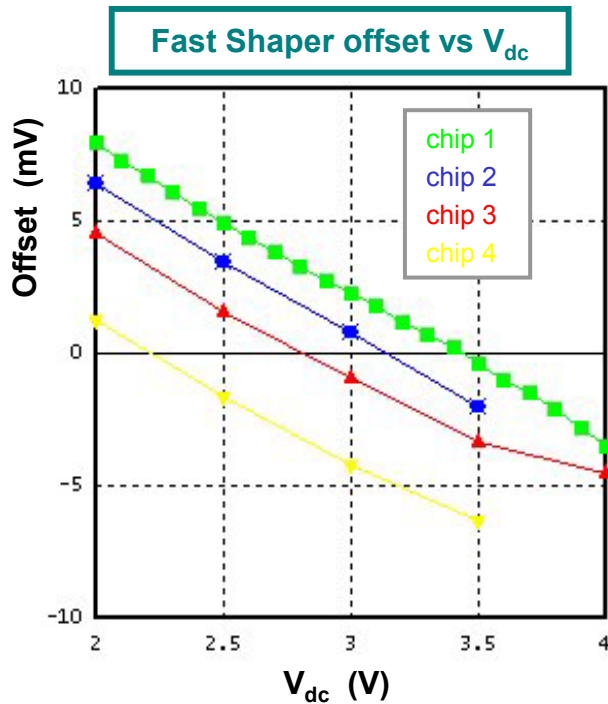
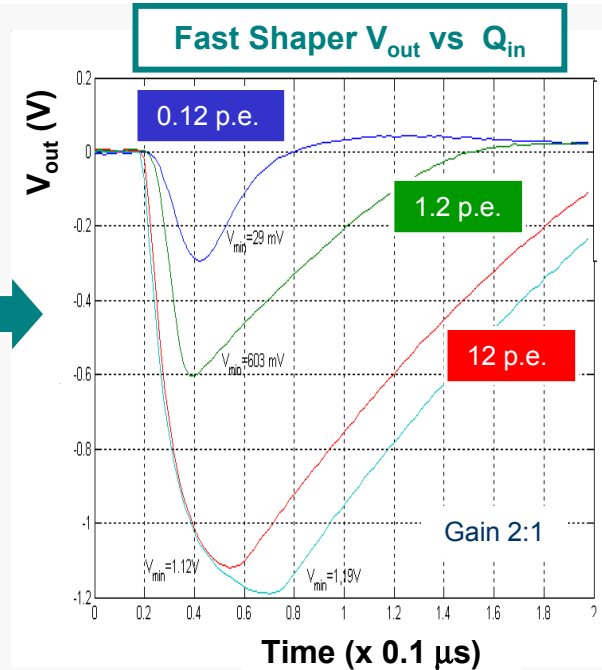
reduce Offset
(pedestal) to 0
at 1st order



Mecano chip: Auto-Trigger

Fast Shaper:

- New Architecture:
 - Differential configuration
 - PMOS input transistor
 - Designed for $V_{DC} = +3V$
- Gain:
 - 250 mV / p.e.
- Speed
 - Rise time $t_R \sim 12$ ns
 - Peak time $t_p \sim 20$ ns

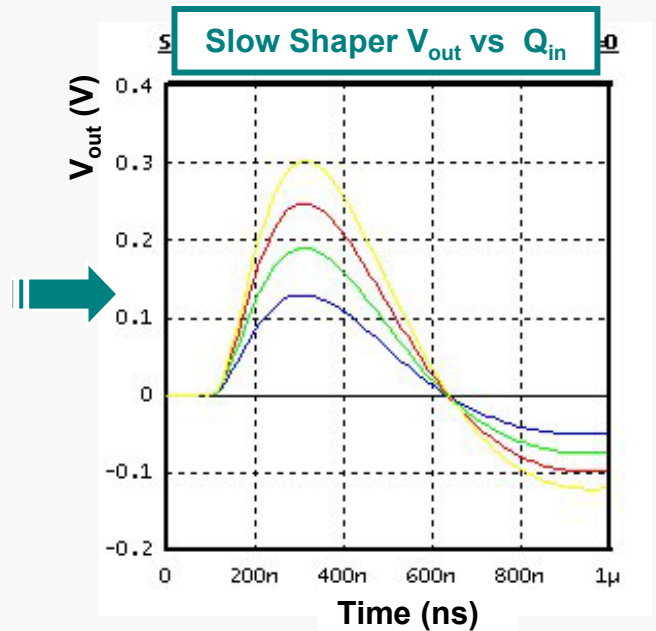


- Noise
 - $G = 1$: 420 μV
 - $G = 2.5$: 850 μV
- Offset spread
 - 4 chips tested
 - Offset slope : 6 mV / V
 - Spread at 3V : -4 / +3 mV (\neq chips !)

Mecano Chip: Slow Shaper

Slow Shaper

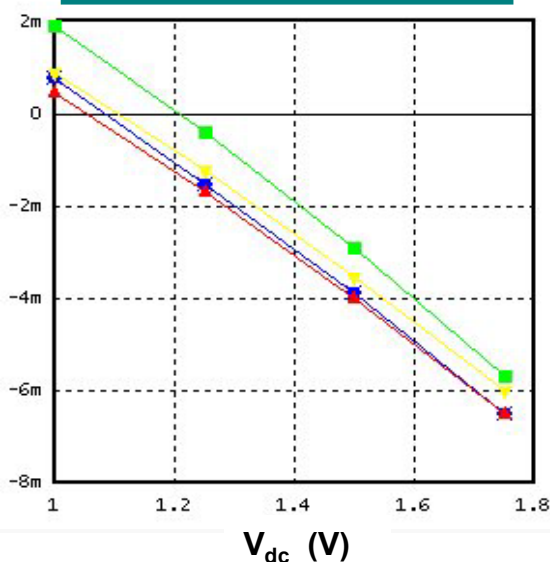
- New Architecture:
 - Differential configuration
 - NPN input differential pair
- Gain
 - $G=1$: 10 mV / p.e.
 - $G=2.5$: 24 mV / pe
- Speed:
 - Peaking time $t_p=187$ ns
 - idem for $G=1$ and $G=2.5$
- Noise:
 - $\sim 500 \mu\text{V}$
- Pedestal spread:
 - 4 chips tested
 - Offset slope: 10 mV/ V
 - Spread at 1.1 V: $\pm 800 \mu\text{V}$



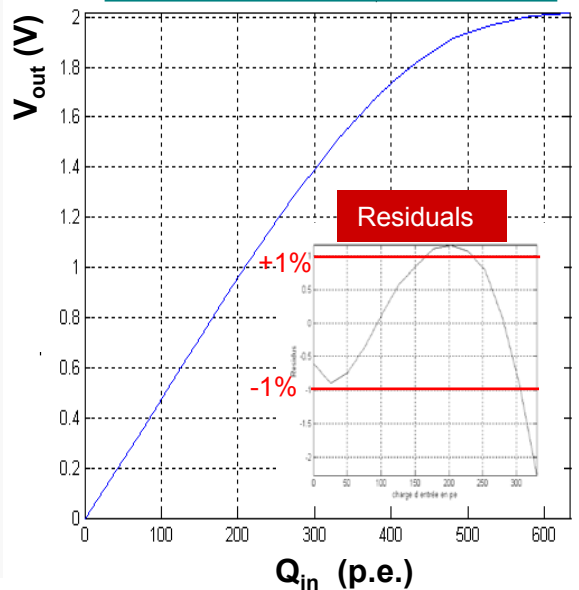
- Linearity:
 - 1% over [1-300] p.e.



Slow Shaper offset vs V_{dc}



Slow Shaper Linearity



Mecano Chip Tests: Summary

Internal note in preparation

	32-channels chip	mecano chip
Auto Trigger:		
Pedestal spread	80 mV	< 4 mV
Noise RMS	1 mV (<< 1.p.e.)	0.5-0.8 mV
Comparator	will be improved	
Fast Shaper t_p	$t_p=35$ ns	$t_p=20$ ns
Fast Shaper Gain	130 mV / p.e.	250 mV / p.e.
Charge meast:		
Dynamic range	[0-80] p.e.	[0-300] p.e.
Gain Correction	Operational (4 bits)	Operational (2 bits)
Pedestal spread	40 mV	< 1 mV
Noise RMS	0.5 mV (<<1.pe.)	0.3 mV (<<1.pe.)
Slow Shaper t_p	$t_p=100$ ns	$t_p=190$ ns
Slow Shaper Gain	16 mV / p.e.	10 mV / p.e.
Cross-talk	O(2%)	--

Pedestal reduced

Increased dynamic range

...on the way to the Final Design

Version 1a Chip

- Conservative Version:
 - no significant change wrt present 32-ch. chip design
- Improvements in the Comparator Design:
 - Separate Voltage alim. (analog / digital)
 - Re-size transistors etc...
- Adjusted parameters in the Shaper
 - No change in the Design
 - Increase t_p (Bern suggestion)

Baseline Version
conservative



– Submitted 27-SEP
– Expected JAN-03

Version 2 (improved) Chip

- Significant improvements:
 - Reduced predestal spread
 - Reduced X-talk
 - Improved for lower signal
- Main new features included:
 - Version 1a comparator
 - Mecano Fast Shaper
 - Mecano Slow Shaper
 - Improved Track & Hold
 - Masking of “dead” channel (not only at trigger level)
 - Register to ID the triggered channel

mostly all the features
tested on the mecano chip



– Submitted JAN-03 (NOV-02 ?)
– Expected MAY-03